A DESIGN STUDY OF HIGH POWER MICROWAVE GaAs FET AMPLIFIER

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DECLARATION

The Work described in this Thesis has not been submitted to any other University for a degree.

Some of the material presented has been published and copies of publications are included in the appropriate sections.

Where use has been made of publications relevant to this work appropriate references have been given.

All other work and conclusions are those of the author unless otherwise stated.

Signed J L Chung

Candidate

SUMMARY

An 8 GHz 10 Watt GaAs FET power amplifier has been developed to replace the TWT in the digital microwave system. For a single bit stream of 91.04 Mbit/s, the residual bit error rate at 40 dBm output power level is 1.0×10^{-32} compared with 1.0×10^{-23} for that of TWT.

For minimizing the non-linearity of the amplifier, the constant gate voltage biasing network has been used and optimized, with the aid of automatic non-linearity measurement technique developed in the thesis. The AM/AM conversion ratio is 0.375 dB/dB and PM/AM is 0.84°/dB at rated output power level of the amplifier.

The total mean-time-between-failure of the amplifier is 350,000 hours. The negative resistance effects in the power GaAs FET is also studied.

ACKNOWLEDGEMENTS

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CHAPTER I INTRODUCTION

The high output power Gallium Arsenide Field Effect Transistor(GaAs FET) was first announced in 1973 by L. Napoli (1) and M. Fukuta (2). Since then, GaAs FET technology has advanced remarkably, and the GaAs FET has become the mainstay for high power solid state microwave devices.

The GaAs FET is a three-terminal device with higher output power and efficiency than other semiconductor devices such as the Gunn and Impatt diodes.

At present, a high power GaAs FET is capable of producing 10 Watts of 1 dB gain compression power with 8 dB gain and 43% power added efficiency at 8 GHz (3). This suggests that GaAs FET amplifier can replace TWTs for some applications.

A TWT(Traveling Wave Tube) is useful microwave amplifier with an excellent performance, and is used in great numbers for terrestrial radio relay systems, satellite communications, and radar systems. However , because the TWT has a relatively short life ,and it operates at high voltage, there has been pressure to develop a solid state power amplifier (SSPA) to replace it(4)-(10).

1.1 Evaluation of GaAs FET (11)

The construction of a typical GaAs FET is shown in Figure 1.1.1. The device operates as follows. When a DC voltage is applied between the gate and the source, the Schottky barrier depletion layer thickness of the gate varies, and this variation is used to control the drain to source current I_{ds}. The equivalent circuit of a GaAs FET in the microwave region is shown in Figure 1.1.2. Using the equivalent circuit parameters, the device current cut-off frequency F_t is expressed as follows;

$$F_t = \frac{g_m}{2\pi(C_{sg} + C_{dg})} \propto \frac{1}{L} \qquad (1.1.1)$$

where L is the gate length.

tne elements (C_{sg} + C_{dg}) represent the total gate-to-channel capacitance; the transconductance g_m relates RF signal current i_{ds} to the voltage across C_{sg}.

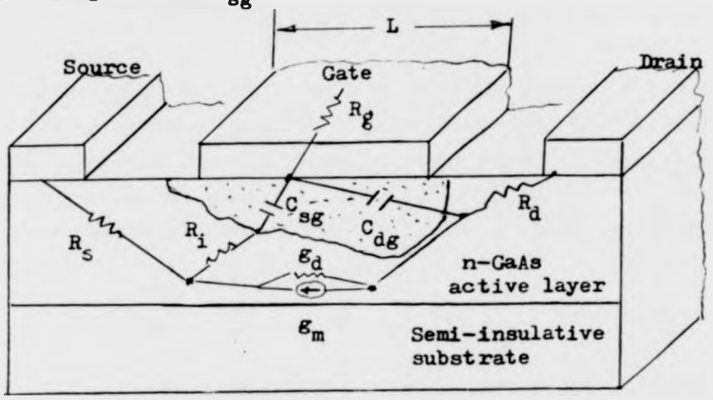
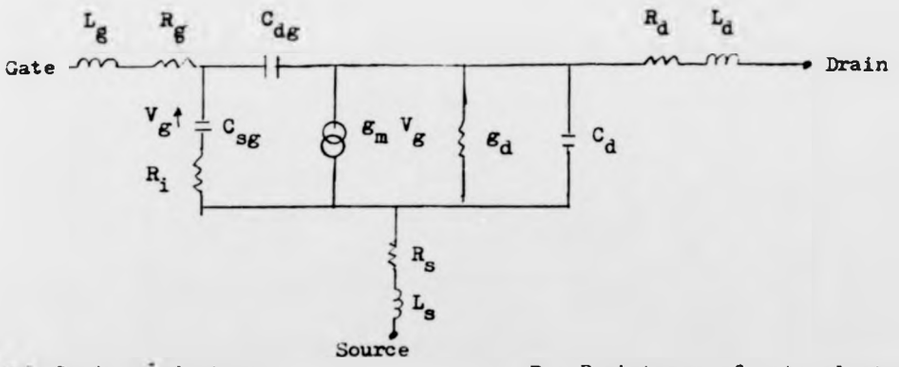


Figure 1.1.1 Cross section of a GaAs FET. Ref.(11)



g_d: Drain conductance
R_i: Channel resistance
R_s: Resistance of source electrode and source contact resistance
R_g: Resistance of gate electrode
L_s: Common source lead inductance
C_{dg}: Miller feedback capacitance

Figure 1.1.2 Equivalent circuit of a FET including parasitic elements. Ref.(11)

As shown in equation (1.1.1), the shorter the gate length(L), the higher the value of f_t.

The basic design approach for a high power FET is to connect several small output cells in parallel, to increase the breakdown voltage between the drain and the source, and to arrange the electrodes in patterns giving the smallest thermal resistance.

The saturation output power (P_{sat}) of a device operating as class A is given by the following formula:

$$P_{sat} = \frac{1}{8} I_{dss}(BV_{ds} - V_{dss}) \qquad (1.1.3)$$

where I_{dss} is the saturation drain current, BV_{ds} is the breakdown voltage between the drain and the source, and V_{dss} is the drain current saturation voltage.

Table 1 shows typical values of the gate geometry (W_g), the breakdown voltage(BV_{ds}), the saturated drain current(I_{dss}), and the output power(P_{1dB}) at 1 dB gain compression for various Fujitsu FETs.

GaAs FET	W_g(μm)	BV_{ds}(V)	I_{dss}(mA)	P_{1dB}(W)
FSX51	300	16	60	60 mW at V_{ds}= 8V f= 8GHz
FSX52	600	16	150	200 mW at V_{ds}=8V f= 8GHz
FLC08	1800	20	250	700 mW at V_{ds}=12V f= 6GHz

Table 1. Typical electrical characteristics of GaAs FETs

1.2 Design philosophy of a TWT replacement amplifier

TWT amplifier have been the backbone of modern communication systems. Providing high gain and high power across a broad bandwidth, they have significantly improved the performance of microwave transmitters and receivers.

But the TWT has the disadvantage of a short life and a high operating voltage.

In developing GaAs FET amplifiers to replace TWTs, design is based on the following points.

1) The amplifier must be compatible with an existing TWT on all points, i.e. the electrical performance.
2) The linearity of the power amplifier is optimized.
3) Automatic level control (ALC) circuit is needed for maintaining a constant gain of the amplifier with variation in temperature.
4) In order to increase the life time of the amplifier, a thermal study in high power devices is required.

1.3 Objectives

This thesis presents a complete design study for an 8 GHz, 10 Watt solid state power amplifier for TWT amplifier replacement in microwave digital radio system. A novel amplifier for this particular application is described in Chapter 5.

The analysis and design of the solid state power amplifiers require that the nonlinear properties of the active devices are well characterized. The third order intercept point is an imaginary power level used to indicate the linearity performance of a "well-behaved" power amplifier (12)(13). Unfortunately, GaAs FET power amplifiers are by no means well-behaved devices (14).

Their third-order intermodulation distortion (IMD_3)curve does not follow the 2:1 relationship with respect to the fundamental signal, nor does their IMD_3 curve follow the 3:1 slope. Consequently, their IMD_3 level connot be calculated in.the conventional manner. In fact, for most GaAs FET power amplifiers the third order intercept point is meaningless(15). A novel automatic non-linearity measurement of GaAs FET power devices or amplifiers is presented in the thesis, which is described in Chapter 2.

Chapter 6 is the thermal study of the GaAs FET power amplifier, a novel concept of the negative resistance due to thermal effect in the GaAs FET power device is described.

A computer program developed by the author is presented in Chapter 3, it is very useful tool for inter-active computer study for the stability properties of a GaAs FET when operating in the linear region.

In Chapter 4 is given the fundamental design method of a linear amplifier (as a driver or pre-amplifier of the power amplifier), using tne Smith chart for approximate design and optimization is done by commercially available CAD technique: COMPACT^{TM} or SUPER-COMPACT^{TM} (16). Large signal behaviour of the power GaAs FET device is also mentioned in this Chapter.

1.4 References

1. L. Napoli et al.:" High power GaAs FET amplifier ..... A multi gate structure," Int. Solid-state Circuit Conf., Dig. Tech. papers, pp. 82ff (1973)
2. M. Fukuta et al.:" Mesh source type microwave power FET," ibid., pp. 84ff.(1973).
3. Fukaya,J., Ishii, M., Matsumoto,M. and Hirano,Y.: " A C-band 10 watt power FET," 1984 IEEE MTT-S Digest, pp.439-441.
4. Sone.,J. et al. :" 14-GHz Band 1 Watt GaAs F.E.T. Amplifier," Electronics Letters 29th March 1979 Vol.15 No.7 pp.212-213.
5. Nakatani, M. et al. :" A 12-GHz 1-W GaAs MESFET Amplifier," IEEE MTT-27,No.12,December 1979,pp.1076-1070.
6. Honjo,K. et al.:"15-Watt Internally Matched GaAs FET and 20-Watt Amplifier Operating at 6-GHz,"NEC R & D No.56,Jan.1980,pp.157-161.
7. Honjo,K. et al.:"A 25-W 5-GHz GaAs FET Amplifier for a Microwave Landing System," IEEE MTT-29,No.6,June 1981,pp.579-582.
8. Goel,J. et al.:" K-Band FET Amplifier for Satellite Downlink," Microwave Journal,Jan. 1984,pp.115-122.
9. Aubert,D. et al.:" Power Amps Replace TWTAs in Satellite Transponsres," Microwave System News April 1983,pp.62-76.
10. Goel,J.:" A K-Band GaAs FET Amplifier with 8.2-W output Power," IEEE MTT-32,No.,March 1984,pp.317-323.
11. Youichi, A. et al.:" High Power GaAs FET Amplifier for TWT replacement," Fujitsu Scientific & Technical Journal, September 1979,pp. 63-82.
12. McVay,F.C.:"Don't Guess the Spurious Level," Electronics Design, Vol.3,pp.70-73(Februry 1967).
13. Fulton,F.F. : "Two-Tone Nonlinearity Testing,The Intercept Point,Pi," 1973 IEEE G-MTT International Microwave Symposium Digest,p.112 (June 4-6 1973).
14. Takayama,Y., et al. :" Nonlinearity and Intermodulation Distortion in Microwave Power GaAs FET Amplifiers," NEC Research & Development No 55 October 1979,pp.1-8.
15. Strid,E.W.,Duder.,T.C.:" Intermodulation Distortion Behavior of GaAs Power FETs," 1978 IEEE MTT-S Digest, pp.135-137.
16. COMPACT Engineering Inc., 1088 Valley View Court, Los Altos, Calif. U.S.A.

CHAPTER 2 AUTOMATIC CHARACTERIZATION FOR THE NONLINEARITY OF THE GaAs FET DEVICES

2.1 GENERAL

It is important to characterize the nonlinearity of behaviour for GaAs FET devices and solid state amplifiers, especially in relation to microwave radio communication systems. The conversion from AM to AM and AM to PM in the active components can contribute significantly to group delay distortion, differential gain, differential phase and consequently intermodulation distortion (1), (2), (3).

The amounts of AM to AM conversion in dB and the degree of AM to PM conversion in an active device normally depend upon the operation level and change with frequency.

The automated measurement system described in this chapter permits measurement of the deviations from linearity of the device under test (D.U.T.) both in gain (delta-gain) and phase (delta-phase) as functions of input power level and frequency.

The changes in biasing voltages and currents due to RF drive are also monitored.

2.2 LINEAR DEVICES

Fig. 2.2 illustrates the meaning of the term "linear device",

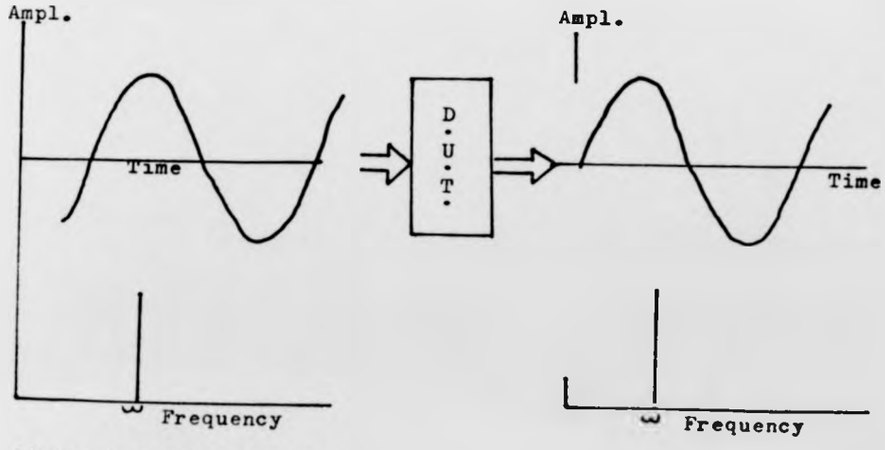


Figure 2.2 Linear device

where: (1) A linear change in the input results in a linear change in the output, and

(2) The output resulting from multiple input signals is the same as the sum of the outputs resulting from individual input signals.

Expressed more simply, it can be said that a sine wave input will result in a sine wave output at the same frequency with nothing changed except possibly amplitude and phase.

2.3 NONLINEAR DEVICES

The output of a nonlinear device is dependent on the level of the input signal as well as the frequency and usually comprises multiple frequencies, as shown in the Figure 2.3.

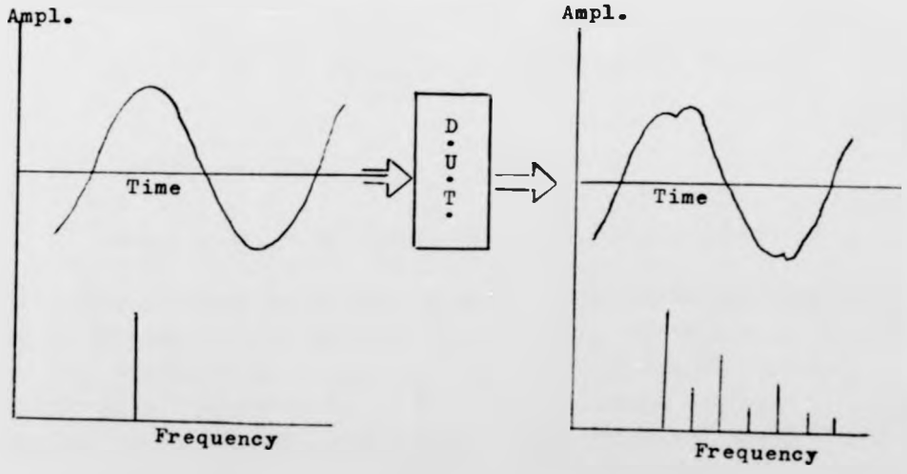
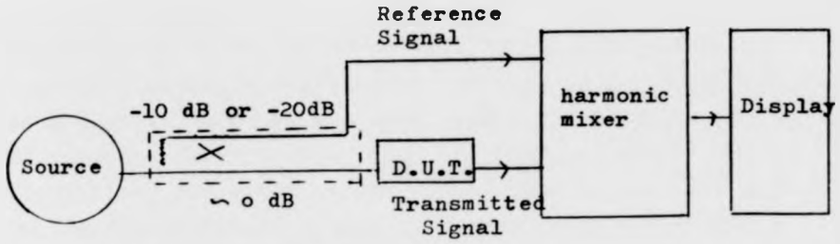
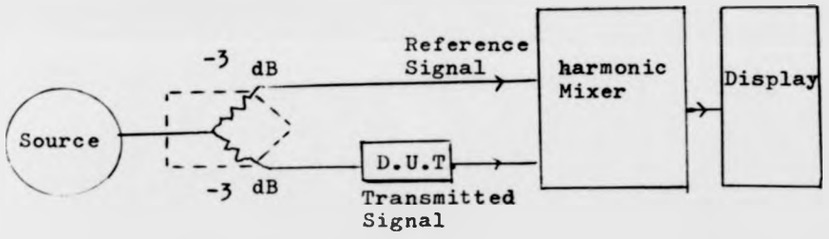


Figure 2.3 Nonlinear device

2.4.1 TRANSMISSION MEASUREMENTS



DIRECTIONAL COUPLER



POWER SPLITTER

Figure 2.4.1 Transmission measurement configurations

Transmission measurements can be made using either a directional coupler or broadband power splitter, as shown in Figure 2.4.1, utilizing the incident signal as a reference. A directional coupler offers the minimum loss (usually $\lesssim$ 2 dB) between the source and the test device, as compared to 3 dB for the power splitter. Power splitters typically are very broadband, having excellent frequency response, and present a good match at the test device input.

Since it is difficult to measure voltages directly at RF or microwave frequencies, a means of converting to low frequency is required, which is the function of harmonic mixing. A mixer, energized by a local oscillator is used to downconvert the RF to a constant IF frequency, which is selected by the IF filter. Together, they act as a tuned, low noise receiver, where the frequency tuning and selectivity are determined by the L.O. frequency and IF filter.

Displaying the ratio of the transmitted to incident signal eliminates the ambiguity caused by source level variations vs. frequency.

2.4.2 MAGNITUDE MEASUREMENTS

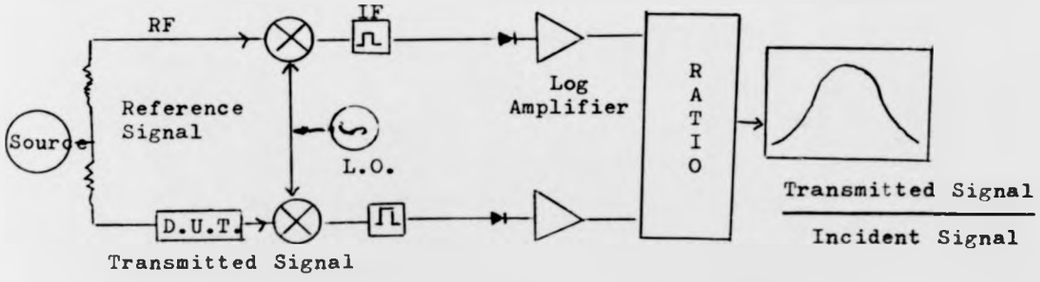


Figure 2.4.2 Magnitude Measurements

Since the relative magnitude and phase information at RF are transferred to a constant IF frequency, as shown in Figure 2.4.2, precision magnitude measurements can be accomplished at a single low frequency.

The magnitude output is usually scaled logarithmically (dB).

2.4.3 PHASE MEASUREMENTS

Phase measurements are accomplished by comparing the phase of the transmitted IF signal with that of the incident IF signal. Note that a reference derived from the incident signal is required for measurements. The phase detector is usually a flip-flop circuit that can measure up to 180° difference in period (phase) of the two IF signals. This results in the traditional display with the 180° phase transitions. Of course, this is entirely equivalent to the Bode plot format where phase is displayed continuously.
(See Figure 2.4.3.)

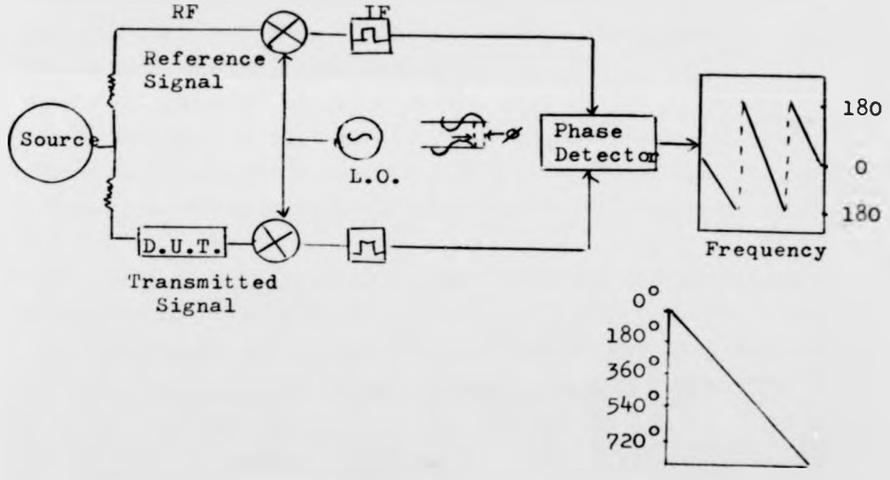


Figure 2.4.3 Phase measurements

2.5. AUTOMATIC MEASUREMENTS FOR DELTA-GAIN AND DELTA-PHASE

Having reviewed the principle of gain and phase measurements, we now take a closer look at delta-gain and delta-phase automatic measurements.

2.5.1 MEASUREMENT SYSTEM DESCRIPTION

The system used to measure delta-gain and delta-phase is shown in Figure 2.5.1. The programmable microwave sweep oscillator hp8350A, with plug-in hp 83592A and solid state amplifier in conjunction with variable attenuator V1, are used to generate a levelled signal of appropriate magnitude in the relevant frequency range. The network analyzer hp8410C with its phase-magnitude display hp8412 is used to measure phase and gain of the D.U.T., facilitated by the incorporation of a computer (e.g. hp9845 or hp9816) linked to the system via an analog-to-digital converter (hp 59313A).

A sample of incident signal from the high directivity coupler, appropriately attenuated, is fed into the reference channel of the hp8411A Harmonic Frequency Converter (H.F.C.). The transmitted signal from the D.U.T. is attenuated before being fed into the test channel of the H.F.C.

Power levels of both input and output signals are monitored by hp436A programmable power meters.

RF drift voltages and currents in the D.U.T. are also measured utilizing the biasing circuit shown in Figure 2.5.3, via an A/D converter to the computer.

2.5.2 RF POWER LEVEL SETTING FOR H.F.C.

It is important to note (See Ref. 5) that :-

1. Reference channel power level (measuring the RF power level into the harmonic frequency converter)must be between -16 and -44 dBm.

2. Test channel power level:- 10 dBm to the system noise level (-78 dBm or below).

3. The test channel cannot be greater than 20 dB over the reference channel. i.e., If the reference channel power level is -40 dBm, the test channel power must be -20 dBm or lower.

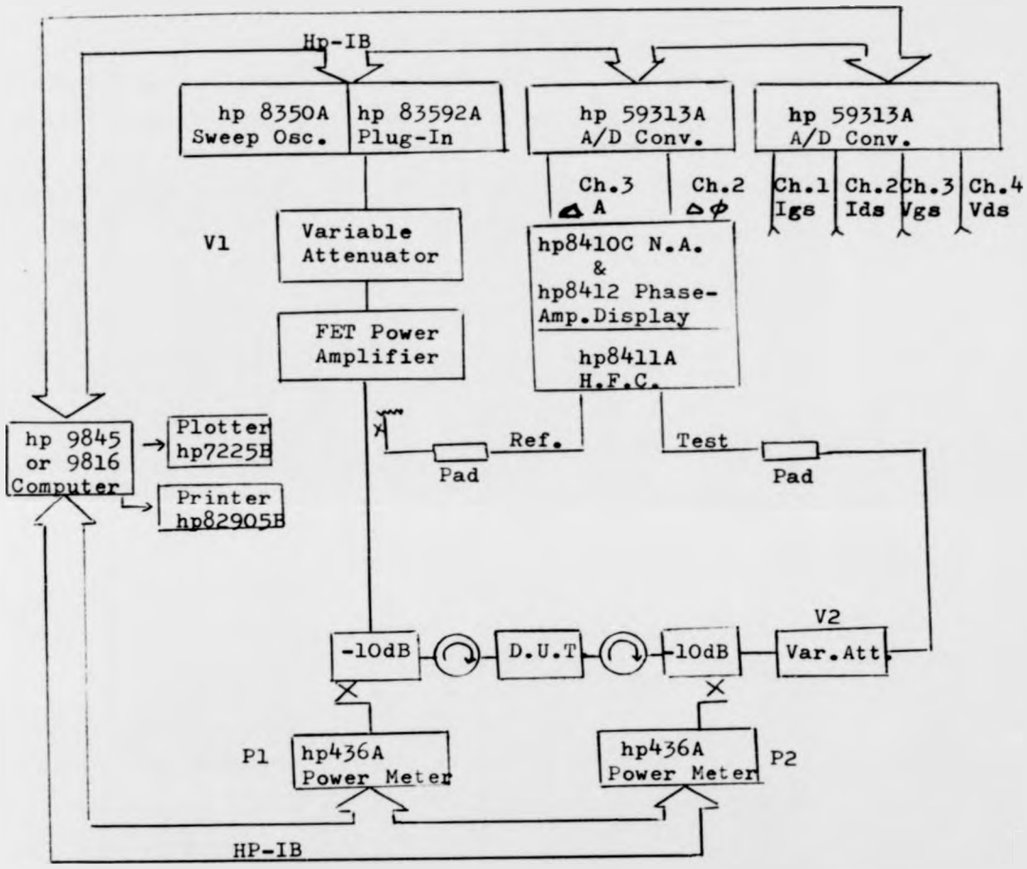


Figure 2.5.1 Automatic delta-gain & delta-phase measurements Set-up.

For maximum dynamic range, the test channel is offset so that the input power level is approximately -10 dBm with the reference channel operating at mid-range or -30 dBm, by placing a 30-dB pad in the test channel and a 3-dB pad in the reference channel, the dynamic range being 47 dB (-57dBm to -10dBm). This is illustrated in Figure 2.5.2.

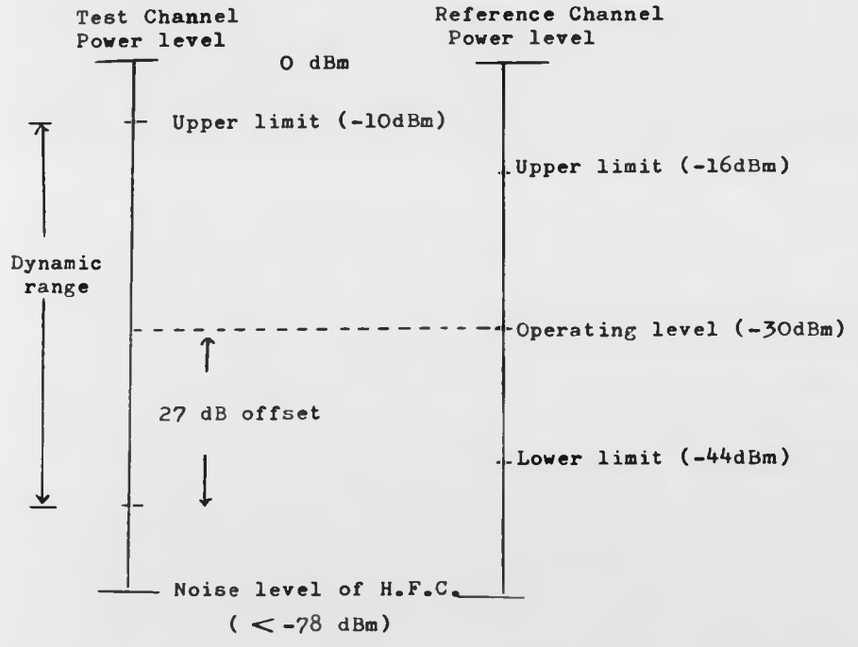


Figure 2.5.2. Power level setting for H.F.C. from page 3-7 of HP Application Note 117-1 (See Ref. 5)

2.5.3 BIAS CIRCUIT FOR GaAs FET AMPLIFIERS

Figure 2.5.3 shows the constant drain current Ids supply. The drain sensing resistor Rd is determined by

$$Rd = \frac{0.5 \quad (Volt)}{(Idss/2) \ (Amp.)} \quad Ohms$$

Idss is the value of the drain currents Ids obtained by making the gate voltage Vgs equal to zero when the device is operating in the pinch-off region.

The voltage drop across Rd is normally maintained at about 0.5 volt, and is utilized as a sensor for providing drain current information to the computer via the A/D converter.

The negative gate voltage supply is obtained via external feedback control of the operational amplifier, the absolute value of gate voltage being set by a 1 KΩ potentiometer. A 100 Ω gate resistor is used as a sensor for monitoring the gate current during system measurements.

Transistor Q1 is turned 'ON' the instant the positive power supply (10.5 volts) is switched on thus clamping the gate bias voltage of the FET to -5 volts to prevent any possible damage to the device.

By using operational amplifiers as an "inverting adder", as shown in Figure 2.5.3 (b) and (c), the absolute values of gate voltage, drain voltage, gate current and drain current can be determined during automatic measurements.

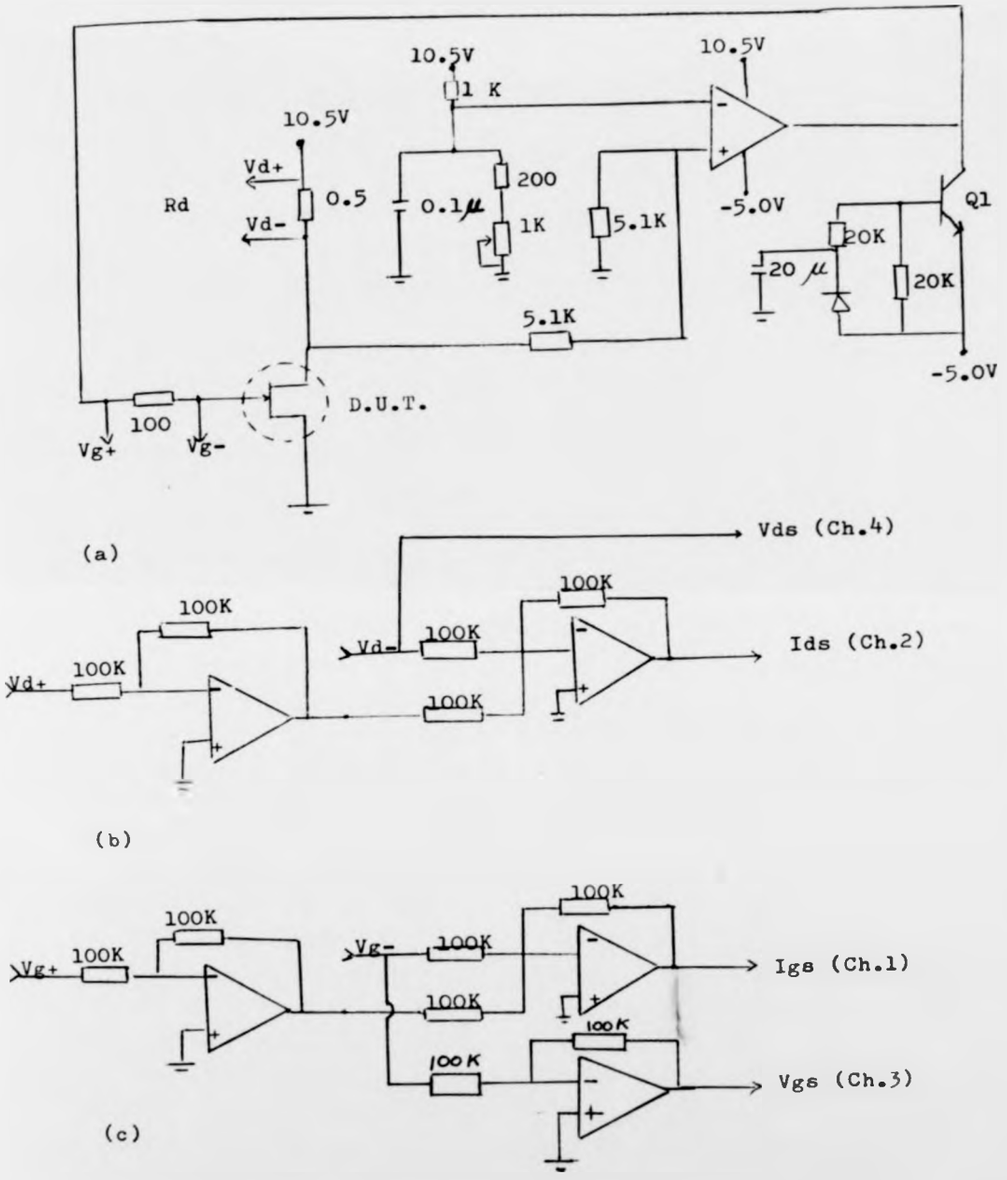


Figure 2.5.3. Bias Circuit for GaAs FET amplifier

2.5.4 METHOD OF MEASUREMENTS

For each measurement, the sweep oscillator is programmed to ' CW ' frequency, and the calibrated power level is stepped within the dynamic range of interest. The magnitude and phase informations from the network analyzer with sensitivity settings of 50mV/dB and 10mV/degree, respectively, are digitized and transferred to the desktop computer.

The hp59313A analog to digital converter has four channels, each channel having four possible input ranges:

LO = Full scale between $\pm$ 1.0 and $\pm$ 1.3 volts
MED = Full scale between $\pm$ 2.5 and $\pm$ 3.5 volts
HI = Full scale between $\pm$ 3.5 and $\pm$ 5.0 volts
HI-HI = Full scale between $\pm$ 7.0 and $\pm$ 10.3 volts

These ranges are selected by a jumper wire placed between pins on the bottom board inside the A/D converter.(7)

The analogue signal in these four possible ranges is converted to 11-bit two's complement binary data before sending to the computer.

In Figure 2.5.1, it is seen that there are six channels required to do system measurements and the following arrangement is made for using two A/D converters:

For A/D converter no. 1 with address number 706, channel 1 is assigned for gate current Igs measurement, setting range 'MED' to 2.5 volts as full scale calibration voltage, the corresponding full scale output of the A/D converter being 1000.

Similarly, channels 2,3 and 4 are assigned for drain current Ids, gate voltage Vgs and drain voltage Vds, setting range 'LO' to 1.0 volt, 'HI' to 5.0 volts and 'HI-HI' to 10.0 volts, respectively for full scale output of the A/D converter set at 1000.

For A/D converter no. 2 with address number 710, only 2 channels are used, i.e., channel 2 and channel 3 are assigned for phase and amplitude measurements. Both channels are set such that range 'LO' has 1.0 volt as its full scale calibration voltage and the full scale output of the A/D converter is also set to 1000.

2.5.5 MEASUREMENT ALGORITHM

In order to maintain the accuracy and repeatability of the measurement results for the 'CW' frequency setting, each measurement is repeated up to 10 times. The measured data can be collected in the form of a matrix:

$$A = \begin{pmatrix} a11 & a12 & a13 & \dots & a1s \\ a21 & a22 & a23 & \dots & a2s \\ a31 & a32 & a33 & \dots & a3s \\ \dots & \dots & \dots & \dots & \dots \\ ar1 & ar2 & ar3 & \dots & ars \end{pmatrix} - \quad (2.5.5.1)$$

The number of rows r is equal to the number of repetition times each 'CW' frequency measurement.

The number of column s represents the number of stepped power levels.

Each number 'ajk' in this matrix is called an element, which is the digitized data from one channel of the A/D converter, the subscripts j and K indicate, respectively, the row and column of the matrix in which the element appears, e.g. 'a11' represents the digitized binary number of the 1st measurement at the starting input power step level, and 'a1s' is that of the last power step level.

For delta-gain and delta-phase evaluations, it is sufficient to measure the change in amplitude and phase corresponding to a change in input power level; it is not necessary to know the absolute values of the amplitude and phase, which can be interpreted by offsetting the 1st column of the matrix A to zeros, and designating the result matrix B, i.e.:

$$B = \begin{pmatrix} a11-a11 & a12-a11 & a13-a11 & \dots & a1s-a11 \\ a21-a21 & a22-a21 & a23-a21 & \dots & a2s-a21 \\ a31-a31 & a32-a31 & a33-a31 & \dots & a3s-a31 \\ \dots & \dots & \dots & \dots & \dots \\ ar1-ar1 & ar2-ar1 & ar3-ar1 & \dots & ars-ar1 \end{pmatrix} \quad - (2.5.5.2)$$

$$= \begin{pmatrix} 0 & b12 & b13 & \dots & b1s \\ 0 & b22 & b23 & \dots & b2s \\ 0 & b32 & b33 & \dots & b3s \\ \dots & \dots & \dots & \dots & \dots \\ 0 & br2 & br3 & \dots & brs \end{pmatrix} \quad - (2.5.5.3)$$

Where : $bjk = ajk - aj1$ — (2.5.5.4)

$(j = 1,r;k = 1,s)$

Taking the sum of elements in each column and dividing by the total number of repetitive measured times, r, yields the average data for each test point, forming a row matrix, namely C , where

$$C = (0, c2, c3, \dots, ck, \dots, cs) \quad - (2.5.5.5)$$

$$\text{and} \quad ck = \left(\sum_{j=1}^{r} bjk \right)/r \quad - (2.5.5.6)$$

$(j = 1,r;k=1,s)$

If one designates the row matrix C for results of calibration measurements, and a row matrix M= (0, m2, m3,...., mk,..., ms) for measurements with a D.U.T. inserted into the system the difference between M and C as D = (mk - ck), then

$$D = (0, d2,d3, \dots, dk..., ds) \quad - (2.5.5.7)$$

$$= (0, m1-c1, m2-c2, m3-c3,...,mk-ck,..., ms-cs)$$

yields the deviation from the linearity of the D.U.T.

Therefore, with the appropriate scaling factors for conversion from a digitized binary number of the A/D converter to the real values of measured parameters, from Equation (2.5.5.7) for delta-gain and delta-phase, it follows that

Delta-gain:

$$G = D/50$$
$$= (\,dk\,)/50 \qquad (k=1,\ s)$$
$$= (0,\ g2,\ g3,\ \ldots,\ gk,\ \ldots,\ gs) \qquad (2.5.5.8)$$

Delta-phase:

$$P = D/10$$
$$= (dk)/10 \quad (k=1,s)$$
$$= (0,\ p2,\ p3,\ \ldots,\ pk,\ldots,\ ps) \qquad (2.5.5.9)$$

A row matrix for absolute input power levels is determined by:

$$I = (i1,\ i2,\ i3,\ \ldots,\ ik,\ldots,\ is) \qquad (2.5.5.10)$$
$$= (\,ik\,) \qquad (k = 1,s)$$

$$ik = Q_1 + \frac{Q2 - Q1}{s - 1} \cdot (k - 1) \qquad (2.5.5.11)$$

where : Q1 = start input power level as desired
Q2 = stop input power level as desired
s = number of steps required for input power level

A row matrix for absolute output power levels is then obtained:

$$O = (o1,\ o2,\ o3,\ \ldots,\ ok,\ \ldots,\ os) \qquad (2.5.5.12)$$
$$= (\,ok\,) \qquad (k = 1,s)$$
$$ok = gk + Gain + Att + ik \qquad (2.5.5.13)$$

where : gk from Eqn. (2.5.5.8)
ik from Eqn. (2.5.5.10)
Gain is the difference between the reading from Power Meters P2 and P1, as in Figure 2.5.1, at the starting input power level.

Att is the precise attenuater value associated with the D.U.T., it any.

The formulae for calculations of gate current Igs, drain current Ids, gate voltage Vgs and drain voltage Vds are:

$$Igs = \frac{25 \times V1}{r} \quad (uA) \qquad (2.5.5.14)$$

$$Ids = \frac{V2}{0.25 \times r} \quad (mA) \qquad (2.5.5.15)$$

$$Vgs = \frac{5 \times V3}{r} \quad (mV) \qquad (2.5.5.16)$$

$$Vds = \frac{V4}{100 \times r} \quad (V) \qquad (2.5.5.17)$$

where V1, V2, V3 and V4 are the digitized binary numbers read from the appropriate channel of the A/D converter.

The added efficiency of the GaAs FET device is defined by:

$$100 \times (10^{\frac{ok}{10}} - 10^{\frac{ik}{10}})/(Ids \times Vds \times 1000 + 10^{\frac{ik}{10}}) \quad \%$$

(k 1,s) (2.5.5.18)

The total D.C. power dissipation in the GaAs FET device is:

$$(1000 \times Ids \times Vds + 10^{\frac{ik}{10}} - 10^{\frac{ok}{10}}) \times 1000 \quad (Watts)$$

(k 1,s) (2.5.5.19)

2.5.6. SYSTEM CONTROL SETTINGS

1. Set up on hp8410C :

(a) 'SOURCE' switch to 'NORMAL'
(b) 'FREQ RANGE' switch to 'AUTO'
(c) 'SWEEP STABILITY' vernier to 'CW'

on hp8412B :

(a) 'PHASE OFFSET POLARITY' to ' + '
(b) 'BW(KHz)' switch to 10

2. Calibration:

(a) Adjust variable attenuator V1 in Figure 2.5.1 to obtain the required input power level of the D.U.T., using power meter P1, starting from approximately 20 dB below the device's saturated level, up to the saturation value. Make sure that the network analyzer 'REF. CHANNEL LEVEL' remains in the 'OPERATE' portion over the entire range, if the needle on this meter moves into the right black portion during the test, reduce the power level; if the needle moves into the left back portion, this could indicate that the system is dropping out of phase lock. Increase the RF power or re-select attenuation via the attenuator pad in the reference channel, then store the calibrated power level in the computer.

(b) Connect the test system back to back (without D.U.T.), adjust 'AMPLITUDE TEST CHANNEL GAIN', 'AMPLITUDE VERNIER', 'PHASE VERNIER' in conjunction with the variable attenuator V2 and attenuator pad in test channel to obtain both magnitude and phase traces on the hp8412 screen.

3. Measurements

Insert the D.U.T. into the system, and leave the 'AMPLITUDE TEST CHANNEL GAIN', 'AMPLITUDE VERNIER' and 'PHASE VERNIER' controls unchanged during the measurements.

In cases when the D.U.T. has high gain, say over 10 dB, it is necessary to have a pad associated with it, as a combined D.U.T., as shown in Figure 2.5.6.

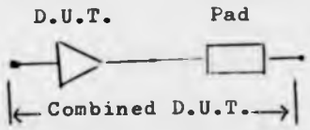


Figure 2.5.6 Combined D.U.T.

The amount of attenuation is approximately equal to the gain of the device under test. As a passive component, the attenuator does not exhibit nonlinearity, no change in amplitude or in phase should occur with a change in input power level.

In cases when the D.U.T. has high gain, say over 10 dB, it is necessary to have a pad associated with it, as a combined D.U.T., as shown in Figure 2.5.6.

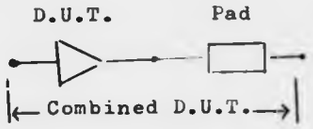
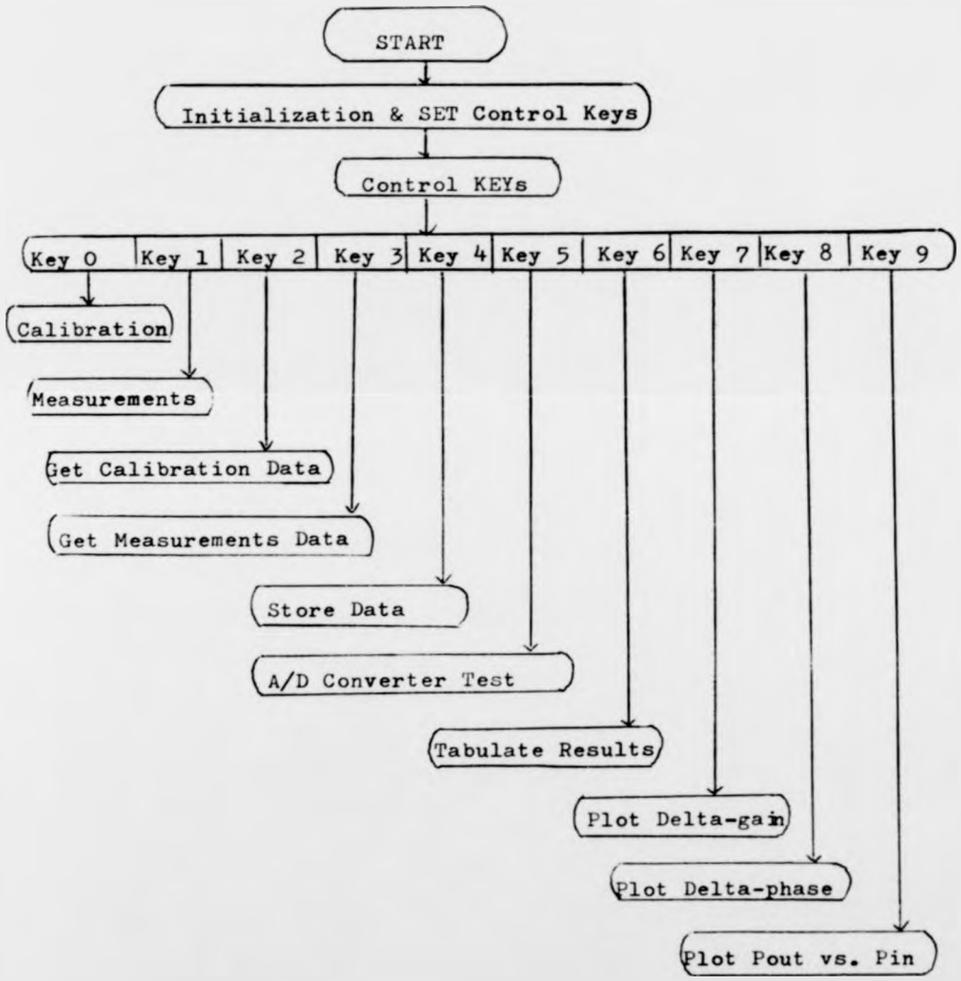


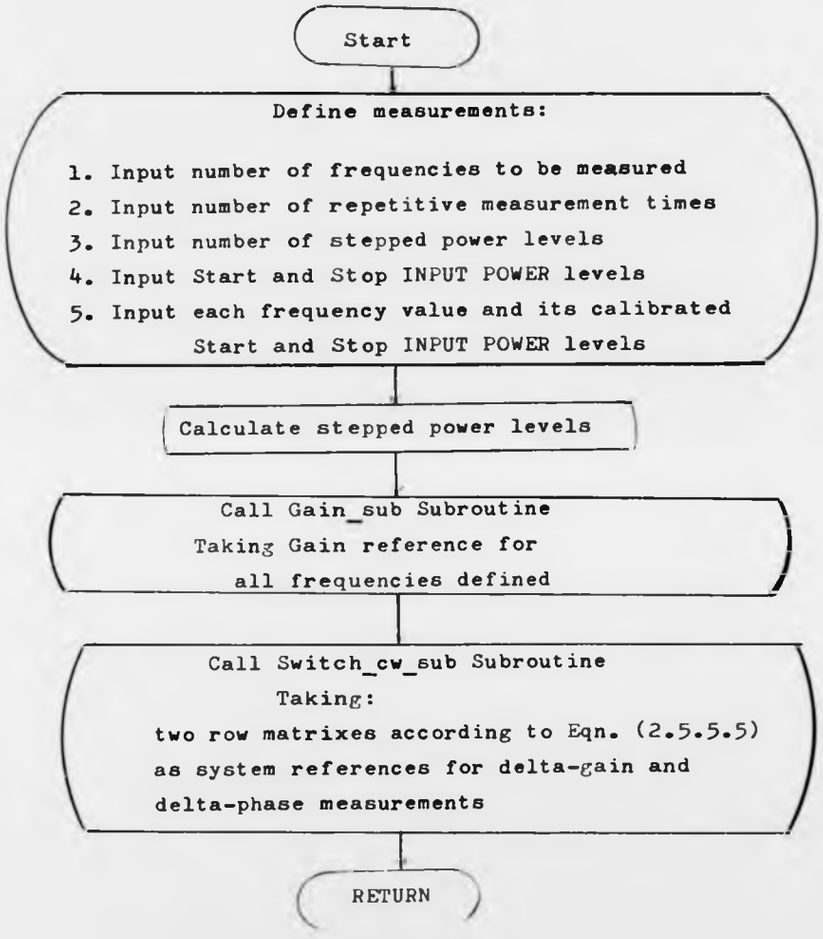
Figure 2.5.6 Combined D.U.T.

The amount of attenuation is approximately equal to the gain of the device under test. As a passive component, the attenuator does not exhibit nonlinearity, no change in amplitude or in phase should occur with a change in input power level.

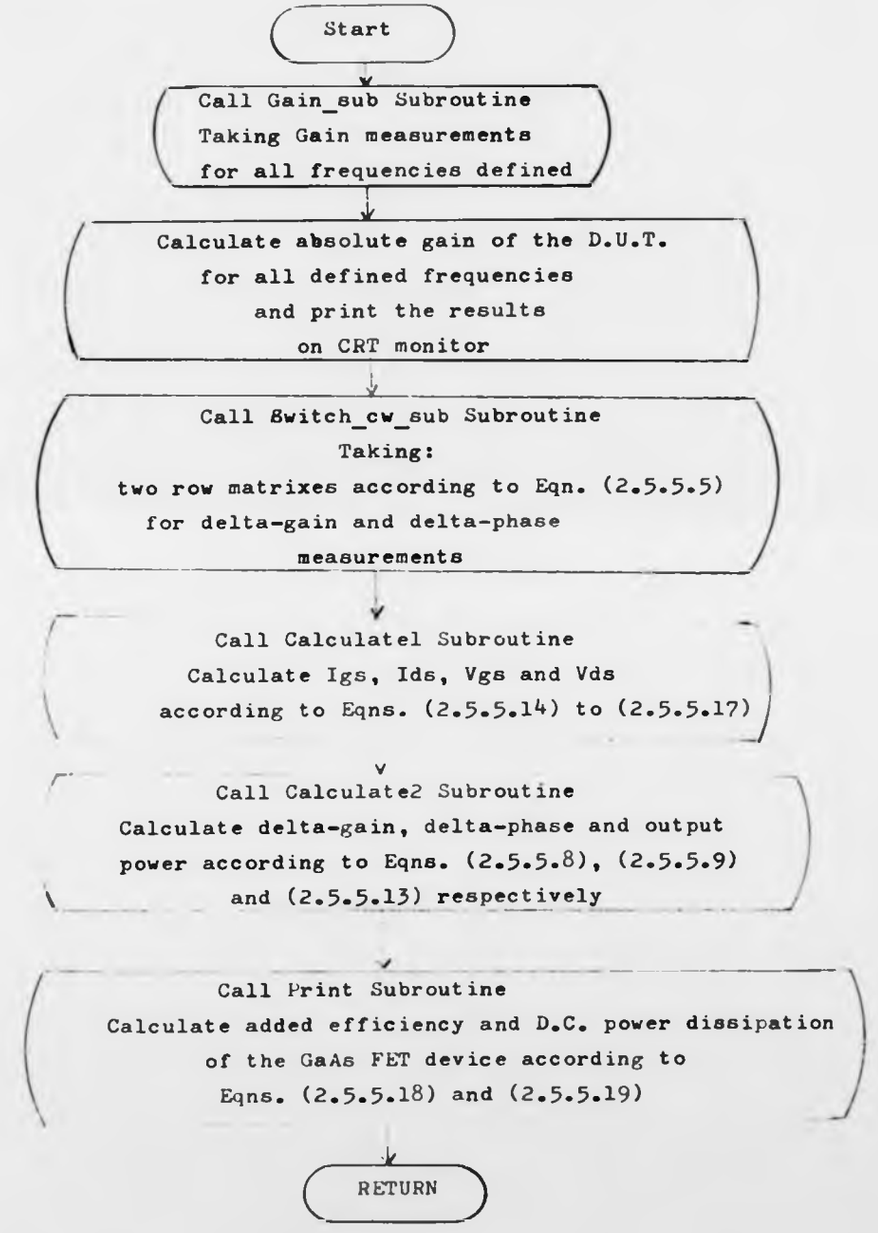
2.6.1 SYSTEM SOFTWARE OVERVIEW



2.6.2 CALIBRATIONS



2.6.3 MEASUREMENTS



2.7 MEASUREMENTS RESULTS

Figure 2.7.0 : The system accuracy test

Figure 2.7.1 : Tabulation for FLM7785-8c (constant Ids) with device efficiency

Figure 2.7.2 : Tabulation for ELM7785-8c (constant Ids) with device D.C. Power dissipation

Figure 2.7.3 : Tabulation for FLM7785-8c (constant Vgs) with device efficiency

Figure 2.7.4 : Tabulation for FLM7785-8c (constant Vgs) with device D.C. power dissipation

Figure 2.7.5 : Plot delta-gain vs. output power (constant Ids)

Figure 2.7.6 : Plot delta-phase vs. output power (constant Ids)

Figure 2.7.7.: Plot delta-gain vs. output power (constant Vgs)

Figure 2.7.8 : Plot delta-phase vs. output power (constant Vgs)

Figure 2.7.9 : Plot pout vs. Pin (constant Ids)

Figure 2.7.10: Plot Pout vs. pin (constant Vgs)

Using computer hp9845c for FLM3742-5

Figure 2.7.11: Plot FLM3742-5 delta-gain vs. input power

Figure 2.7.12: Plot FLM3742-5 delta-phase vs. input power

Figure 2.7.0 System Accuracy Test

FREQ (GHz) = 7.7 GAIN (dBm) = .02

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	22.02	0.00	0.00	0.00	0.00	0.00	0.00	0.00
23.09	23.12	.01	-.07	0.00	0.00	0.00	0.00	0.00
24.18	24.20	-0.00	-.04	0.00	0.00	0.00	0.00	0.00
25.27	25.30	.01	.07	0.00	0.00	0.00	0.00	0.00
26.36	26.39	.01	-.07	0.00	0.00	0.00	0.00	0.00
27.45	27.47	-0.00	.01	0.00	0.00	0.00	0.00	0.00
28.55	28.57	0.00	-.03	0.00	0.00	0.00	0.00	0.00
29.64	29.65	-0.00	-.11	0.00	0.00	0.00	0.00	0.00
30.73	30.75	0.00	-.01	0.00	0.00	0.00	0.00	0.00
31.82	31.84	0.00	-.07	0.00	0.00	0.00	0.00	0.00
32.91	32.92	-.01	-.11	0.00	0.00	0.00	0.00	0.00
34.00	34.01	-.01	-.07	0.00	0.00	0.00	0.00	0.00

FREQ (GHz) = 8 GAIN (dBm) = 0

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	22.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00
23.09	23.09	-.01	-.03	0.00	0.00	0.00	0.00	0.00
24.18	24.19	.01	-.03	0.00	0.00	0.00	0.00	0.00
25.27	25.27	0.00	-.06	0.00	0.00	0.00	0.00	0.00
26.36	26.37	0.00	-.04	0.00	0.00	0.00	0.00	0.00
27.45	27.45	0.00	-.09	0.00	0.00	0.00	0.00	0.00
28.55	28.54	-0.00	0.00	0.00	0.00	0.00	0.00	0.00
29.64	29.63	-0.00	-.10	0.00	0.00	0.00	0.00	0.00
30.73	30.73	0.00	-.04	0.00	0.00	0.00	0.00	0.00
31.82	31.82	.01	.01	0.00	0.00	0.00	0.00	0.00
32.91	32.91	-0.00	-.04	0.00	0.00	0.00	0.00	0.00
34.00	34.00	0.00	-.07	0.00	0.00	0.00	0.00	0.00

FREQ (GHz) = 8.3 GAIN (dBm) = .03

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	22.03	0.00	0.00	0.00	0.00	0.00	0.00	0.00
23.09	23.11	-.01	.04	0.00	0.00	0.00	0.00	0.00
24.18	24.21	0.00	-.04	0.00	0.00	0.00	0.00	0.00
25.27	25.31	0.00	.01	0.00	0.00	0.00	0.00	0.00
26.36	26.40	.01	-.07	0.00	0.00	0.00	0.00	0.00
27.45	27.47	-.01	.09	0.00	0.00	0.00	0.00	0.00
28.55	28.59	.01	.01	0.00	0.00	0.00	0.00	0.00
29.64	29.66	-0.00	.07	0.00	0.00	0.00	0.00	0.00
30.73	30.76	0.00	0.00	0.00	0.00	0.00	0.00	0.00
31.82	31.85	0.00	.03	0.00	0.00	0.00	0.00	0.00
32.91	32.94	0.00	0.00	0.00	0.00	0.00	0.00	0.00
34.00	34.03	0.00	.04	0.00	0.00	0.00	0.00	0.00

Figure 2.7.1 FLM7785-8C (Constant Ids) with device efficiency

15:29:18
FREQ (GHz) = 7.7 GAIN (dBm) = 7.36

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	29.36	0.00	0.00	-25.00	-1068.57	2108.00	10.10	3.28
23.09	30.42	-.03	-.14	-25.00	-1073.57	2108.00	10.10	4.18
24.18	31.47	-.07	-.01	-25.00	-1080.00	2108.00	10.10	5.29
25.27	32.53	-.10	.21	-32.14	-1087.14	2108.00	10.10	6.72
26.36	33.57	-.15	.46	-50.00	-1098.57	2108.00	10.10	8.48
27.45	34.58	-.23	.89	-50.00	-1116.43	2108.00	10.10	10.59
28.55	35.55	-.35	1.33	-75.00	-1142.86	2108.00	10.10	13.06
29.64	36.47	-.53	1.91	-96.43	-1178.57	2108.00	10.10	15.82
30.73	37.32	-.77	2.83	-128.57	-1227.86	2108.00	10.10	18.75
31.82	38.07	-1.11	3.70	-182.14	-1295.00	2108.00	10.10	21.46
32.91	38.70	-1.57	4.46	-260.71	-1381.43	2108.00	10.10	23.46
34.00	39.19	-2.17	5.13	-421.43	-1494.29	2108.00	10.10	24.30

FREQ (GHz) = 8 GAIN (dBm) = 8.34

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	30.34	0.00	0.00	-25.00	-1075.71	2108.00	10.10	4.30
23.09	31.40	-.03	.13	-50.00	-1082.86	2108.00	10.10	5.47
24.18	32.46	-.06	.37	-50.00	-1090.71	2108.00	10.10	6.97
25.27	33.51	-.11	.79	-50.00	-1105.00	2108.00	10.10	8.81
26.36	34.52	-.19	1.26	-75.00	-1125.00	2108.00	10.10	11.03
27.45	35.51	-.29	1.91	-100.00	-1153.57	2108.00	10.10	13.71
28.55	36.42	-.46	2.86	-125.00	-1192.86	2108.00	10.10	16.69
29.64	37.26	-.72	3.99	-175.00	-1250.00	2108.00	10.10	19.81
30.73	37.98	-1.09	5.44	-246.43	-1328.57	2108.00	10.10	22.68
31.82	38.54	-1.62	6.84	-378.57	-1432.14	2108.00	10.10	24.67
32.91	38.94	-2.31	7.94	-614.29	-1562.14	2108.00	10.10	25.28
34.00	39.21	-3.13	8.90	-1042.86	-1734.29	2108.00	10.10	24.46

FREQ (GHz) = 8.3 GAIN (dBm) = 8.56

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	30.56	0.00	0.00	-50.00	-1075.71	2108.00	10.10	4.56
23.09	31.63	-.03	.26	-50.00	-1085.00	2108.00	10.10	5.82
24.18	32.68	-.06	.46	-50.00	-1095.00	2108.00	10.10	7.39
25.27	33.73	-.10	.90	-75.00	-1110.71	2108.00	10.10	9.35
26.36	34.76	-.16	1.43	-100.00	-1137.14	2108.00	10.10	11.79
27.45	35.75	-.26	2.30	-125.00	-1180.00	2108.00	10.10	14.67
28.55	36.70	-.41	3.21	-192.86	-1235.00	2108.00	10.10	18.00
29.64	37.55	-.64	4.29	-271.43	-1305.71	2108.00	10.10	21.49
30.73	38.29	-1.00	5.23	-414.29	-1393.57	2108.00	10.10	24.73
31.82	38.84	-1.53	6.07	-678.57	-1503.57	2108.00	10.10	26.93
32.91	39.25	-2.22	6.66	-1275.00	-1681.43	2108.00	10.10	27.76
34.00	39.43	-3.13	7.03	-2792.86	-2029.29	2108.00	10.10	26.26

Figure 2.7.2 FLM7785-8C (Constant Ids) with device d.c. power

FREQ (GHz) = 7.7 GAIN (dBm) = 7.36

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Tr.D.C.Pw. (Watts)
22.00	29.36	0.00	0.00	-25.00	-1068.57	2108.00	10.10	20.59
23.09	30.42	-.03	-.14	-25.00	-1073.57	2108.00	10.10	20.40
24.18	31.47	-.07	-.01	-25.00	-1080.00	2108.00	10.10	20.16
25.27	32.53	-.10	.21	-32.14	-1087.14	2108.00	10.10	19.84
26.36	33.57	-.15	.46	-50.00	-1098.57	2108.00	10.10	19.45
27.45	34.58	-.23	.89	-50.00	-1116.43	2108.00	10.10	18.99
28.55	35.55	-.35	1.33	-75.00	-1142.86	2108.00	10.10	18.42
29.64	36.47	-.53	1.91	-96.43	-1178.57	2108.00	10.10	17.78
30.73	37.32	-.77	2.83	-128.57	-1227.86	2108.00	10.10	17.08
31.82	38.07	-1.11	3.70	-182.14	-1295.00	2108.00	10.10	16.40
32.91	38.70	-1.57	4.46	-260.71	-1381.43	2108.00	10.10	15.84
34.00	39.19	-2.17	5.13	-421.43	-1494.29	2108.00	10.10	15.51

FREQ (GHz) = 8 GAIN (dBm) = 8.34

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Tr.D.C.Pw. (Watts)
22.00	30.34	0.00	0.00	-25.00	-1075.71	2108.00	10.10	20.37
23.09	31.40	-.03	.13	-50.00	-1082.86	2108.00	10.10	20.12
24.18	32.46	-.06	.37	-50.00	-1090.71	2108.00	10.10	19.80
25.27	33.51	-.11	.79	-50.00	-1105.00	2108.00	10.10	19.39
26.36	34.52	-.19	1.26	-75.00	-1125.00	2108.00	10.10	18.90
27.45	35.51	-.29	1.91	-100.00	-1153.57	2108.00	10.10	18.30
28.55	36.42	-.46	2.86	-125.00	-1192.86	2108.00	10.10	17.62
29.64	37.26	-.72	3.99	-175.00	-1250.00	2108.00	10.10	16.90
30.73	37.98	-1.09	5.44	-246.43	-1328.57	2108.00	10.10	16.19
31.82	38.54	-1.62	6.84	-378.57	-1432.14	2108.00	10.10	15.66
32.91	38.94	-2.31	7.94	-614.29	-1562.14	2108.00	10.10	15.41
34.00	39.21	-3.13	8.90	-1042.86	-1734.29	2108.00	10.10	15.47

FREQ (GHz) = 8.3 GAIN (dBm) = 8.56

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Tr.D.C.Pw. (Watts)
22.00	30.56	0.00	0.00	-50.00	-1075.71	2108.00	10.10	20.32
23.09	31.63	-.03	.26	-50.00	-1085.00	2108.00	10.10	20.04
24.18	32.68	-.06	.46	-50.00	-1095.00	2108.00	10.10	19.70
25.27	33.73	-.10	.90	-75.00	-1110.71	2108.00	10.10	19.28
26.36	34.76	-.16	1.43	-100.00	-1137.14	2108.00	10.10	18.73
27.45	35.75	-.26	2.30	-125.00	-1180.00	2108.00	10.10	18.09
28.55	36.70	-.41	3.21	-192.86	-1235.00	2108.00	10.10	17.33
29.64	37.55	-.64	4.29	-271.43	-1305.71	2108.00	10.10	16.52
30.73	38.29	-1.00	5.23	-414.29	-1393.57	2108.00	10.10	15.74
31.82	38.84	-1.53	6.07	-678.57	-1503.57	2108.00	10.10	15.15
32.91	39.25	-2.22	6.66	-1275.00	-1681.43	2108.00	10.10	14.84
34.00	39.43	-3.13	7.03	-2792.86	-2029.29	2108.00	10.10	15.04

Figure 2.7.3 FLM7785-8C (Constant Vgs) with device efficiency

FREQ (GHz) = 7.7 GAIN (dBm) = 7.3

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	29.30	0.00	0.00	-42.86	-1057.14	2128.00	10.10	3.20
23.09	30.36	-.03	-.14	-50.00	-1056.43	2135.43	10.09	4.06
24.18	31.44	-.04	-.04	-50.00	-1055.71	2143.43	10.09	5.17
25.27	32.50	-.07	.16	-50.00	-1055.00	2155.43	10.09	6.53
26.36	33.56	-.10	.37	-50.00	-1055.00	2172.00	10.08	8.24
27.45	34.62	-.14	.77	-67.86	-1055.00	2198.86	10.07	10.30
28.55	35.67	-.18	1.11	-75.00	-1050.71	2236.57	10.06	12.80
29.64	36.67	-.26	1.51	-103.57	-1047.14	2289.71	10.04	15.60
30.73	37.66	-.37	2.13	-142.86	-1040.71	2360.57	10.02	18.74
31.82	38.56	-.55	2.43	-192.86	-1032.14	2453.14	9.98	21.78
32.91	39.29	-.92	2.31	-282.14	-1018.57	2550.86	9.95	23.89
34.00	39.77	-1.53	2.04	-271.43	-1020.00	2599.43	9.93	24.60

FREQ (GHz) = 8 GAIN (dBm) = 8.28

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	30.28	0.00	0.00	-50.00	-1055.00	2133.71	10.09	4.19
23.09	31.37	-.01	.14	-50.00	-1055.00	2144.57	10.09	5.34
24.18	32.44	-.02	.39	-50.00	-1055.00	2160.57	10.09	6.77
25.27	33.51	-.04	.66	-75.00	-1054.29	2180.00	10.08	8.55
26.36	34.57	-.07	1.10	-75.00	-1050.00	2208.57	10.07	10.72
27.45	35.63	-.11	1.53	-100.00	-1049.29	2245.14	10.06	13.38
28.55	36.65	-.17	2.11	-125.00	-1045.00	2299.43	10.04	16.43
29.64	37.62	-.29	2.59	-175.00	-1035.00	2376.57	10.01	19.69
30.73	38.49	-.52	2.93	-250.00	-1020.71	2476.57	9.98	22.71
31.82	39.14	-.96	2.71	-378.57	-1000.71	2586.86	9.94	24.53
32.91	39.59	-1.60	2.09	-421.43	-993.57	2662.29	9.91	25.23
34.00	39.83	-2.45	2.86	53.57	-1075.71	2589.71	9.94	25.16

FREQ (GHz) = 8.3 GAIN (dBm) = 8.52

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Eff. (%)
22.00	30.52	0.00	0.00	-50.00	-1055.00	2134.29	10.09	4.46
23.09	31.60	-.01	.16	-50.00	-1055.00	2146.86	10.09	5.67
24.18	32.68	-.02	.39	-75.00	-1055.00	2162.29	10.08	7.21
25.27	33.76	-.04	.76	-75.00	-1050.00	2185.14	10.08	9.11
26.36	34.83	-.05	1.14	-100.00	-1050.00	2222.86	10.06	11.45
27.45	35.89	-.09	1.67	-125.00	-1043.57	2277.14	10.04	14.18
28.55	36.91	-.15	2.00	-175.00	-1035.00	2348.00	10.02	17.32
29.64	37.82	-.34	2.16	-250.00	-1025.00	2428.00	9.99	20.37
30.73	38.55	-.70	1.86	-346.43	-1005.71	2512.00	9.97	22.80
31.82	39.11	-1.23	1.03	-475.00	-982.86	2595.43	9.94	24.26
32.91	39.49	-1.94	.57	-300.00	-1015.00	2582.86	9.94	25.09
34.00	39.65	-2.87	1.94	528.57	-1160.00	2440.00	9.99	24.94

Figure 2.7.4 FLM7785-8C (Constant Vgs) with device d.c. power

FREQ (GHz) = 7.7 GAIN (dBm) = 7.3

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Tr.D.C.Pw. (Watts)
22.00	29.30	0.00	0.00	-42.86	-1057.14	2128.00	10.10	20.80
23.09	30.36	-.03	-.14	-50.00	-1056.43	2135.43	10.09	20.67
24.18	31.44	-.04	-.04	-50.00	-1055.71	2143.43	10.09	20.50
25.27	32.50	-.07	.16	-50.00	-1055.00	2155.43	10.09	20.31
26.36	33.56	-.10	.37	-50.00	-1055.00	2172.00	10.08	20.05
27.45	34.62	-.14	.77	-67.86	-1055.00	2198.86	10.07	19.80
28.55	35.67	-.18	1.11	-75.00	-1050.71	2236.57	10.06	19.53
29.64	36.67	-.26	1.51	-103.57	-1047.14	2289.71	10.04	19.26
30.73	37.66	-.37	2.13	-142.86	-1040.71	2360.57	10.02	19.00
31.82	38.56	-.55	2.43	-192.86	-1032.14	2453.14	9.98	18.83
32.91	39.29	-.92	2.31	-282.14	-1018.57	2550.86	9.95	18.85
34.00	39.77	-1.53	2.04	-271.43	-1020.00	2599.43	9.93	18.85

FREQ (GHz) = 8 GAIN (dBm) = 8.28

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Tr.D.C.Pw. (Watts)
22.00	30.28	0.00	0.00	-50.00	-1055.00	2133.71	10.09	20.63
23.09	31.37	-.01	.14	-50.00	-1055.00	2144.57	10.09	20.47
24.18	32.44	-.02	.39	-50.00	-1055.00	2160.57	10.09	20.30
25.27	33.51	-.04	.66	-75.00	-1054.29	2180.00	10.08	20.07
26.36	34.57	-.07	1.10	-75.00	-1050.00	2208.57	10.07	19.81
27.45	35.63	-.11	1.53	-100.00	-1049.29	2245.14	10.06	19.49
28.55	36.65	-.17	2.11	-125.00	-1045.00	2299.43	10.04	19.18
29.64	37.62	-.29	2.59	-175.00	-1035.00	2376.57	10.01	18.93
30.73	38.49	-.52	2.93	-250.00	-1020.71	2476.57	9.98	18.84
31.82	39.14	-.96	2.71	-378.57	-1000.71	2586.86	9.94	19.03
32.91	39.59	-1.60	2.09	-421.43	-993.57	2662.29	9.91	19.23
34.00	39.83	-2.45	2.86	53.57	-1075.71	2589.71	9.94	18.63

FREQ (GHz) = 8.3 GAIN (dBm) = 8.52

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)	Tr.D.C.Pw. (Watts)
22.00	30.52	0.00	0.00	-50.00	-1055.00	2134.29	10.09	20.58
23.09	31.60	-.01	.16	-50.00	-1055.00	2146.86	10.09	20.42
24.18	32.68	-.02	.39	-75.00	-1055.00	2162.29	10.08	20.21
25.27	33.76	-.04	.76	-75.00	-1050.00	2185.14	10.08	19.99
26.36	34.83	-.05	1.14	-100.00	-1050.00	2222.86	10.06	19.76
27.45	35.89	-.09	1.67	-125.00	-1043.57	2277.14	10.04	19.55
28.55	36.91	-.15	2.00	-175.00	-1035.00	2348.00	10.02	19.33
29.64	37.82	-.34	2.16	-250.00	-1025.00	2428.00	9.99	19.13
30.73	38.55	-.70	1.86	-346.43	-1005.71	2512.00	9.97	19.07
31.82	39.11	-1.23	1.03	-475.00	-982.86	2595.43	9.94	19.17
32.91	39.49	-1.94	.57	-300.00	-1015.00	2582.86	9.94	18.74
34.00	39.65	-2.87	1.94	528.57	-1160.00	2440.00	9.99	17.67

FIGURE 2.7.5 DELTA-GAIN v.s. OUTPUT POWER

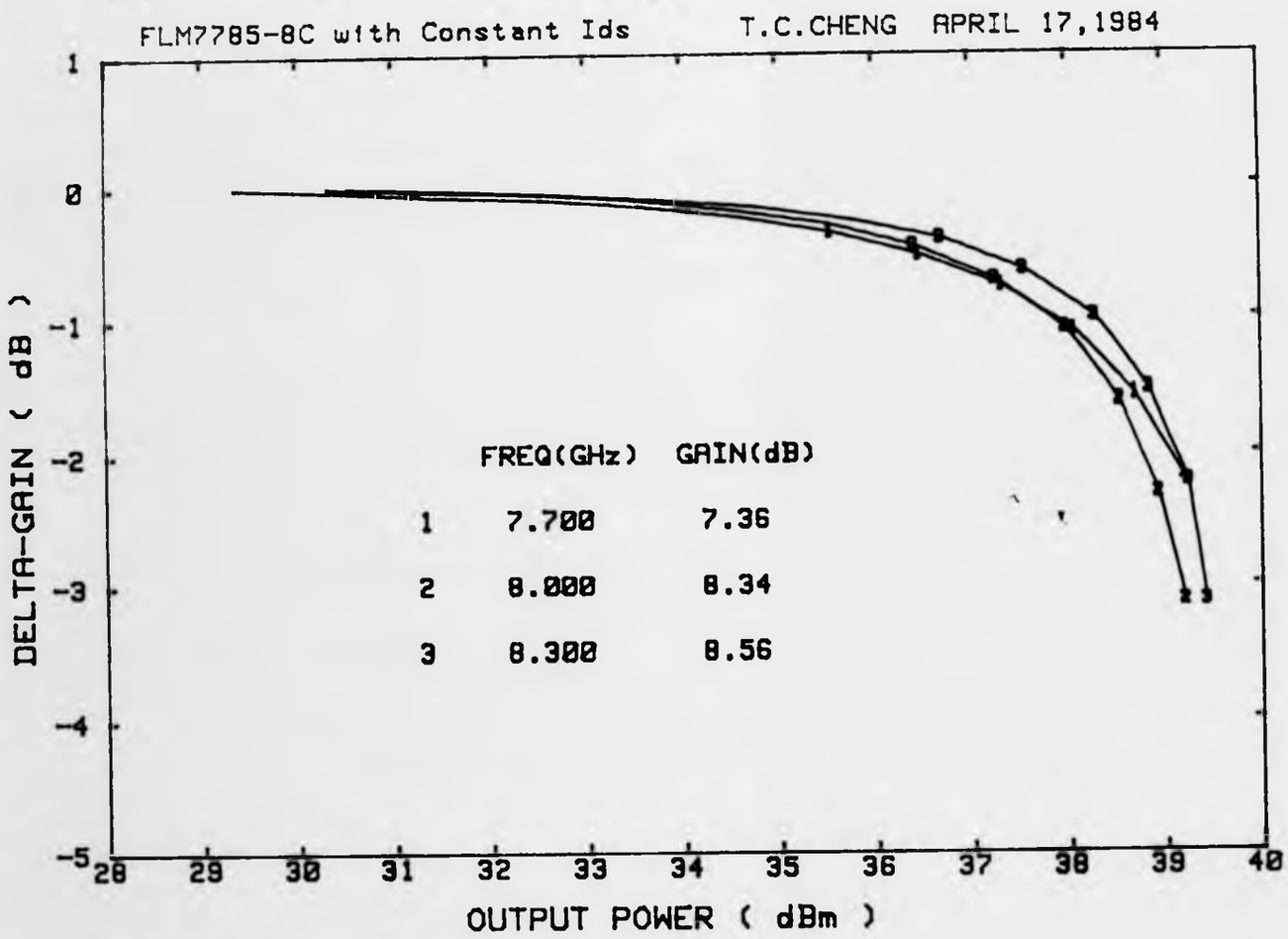


FIGURE 2.7.5 DELTA-GAIN v.s. OUTPUT POWER

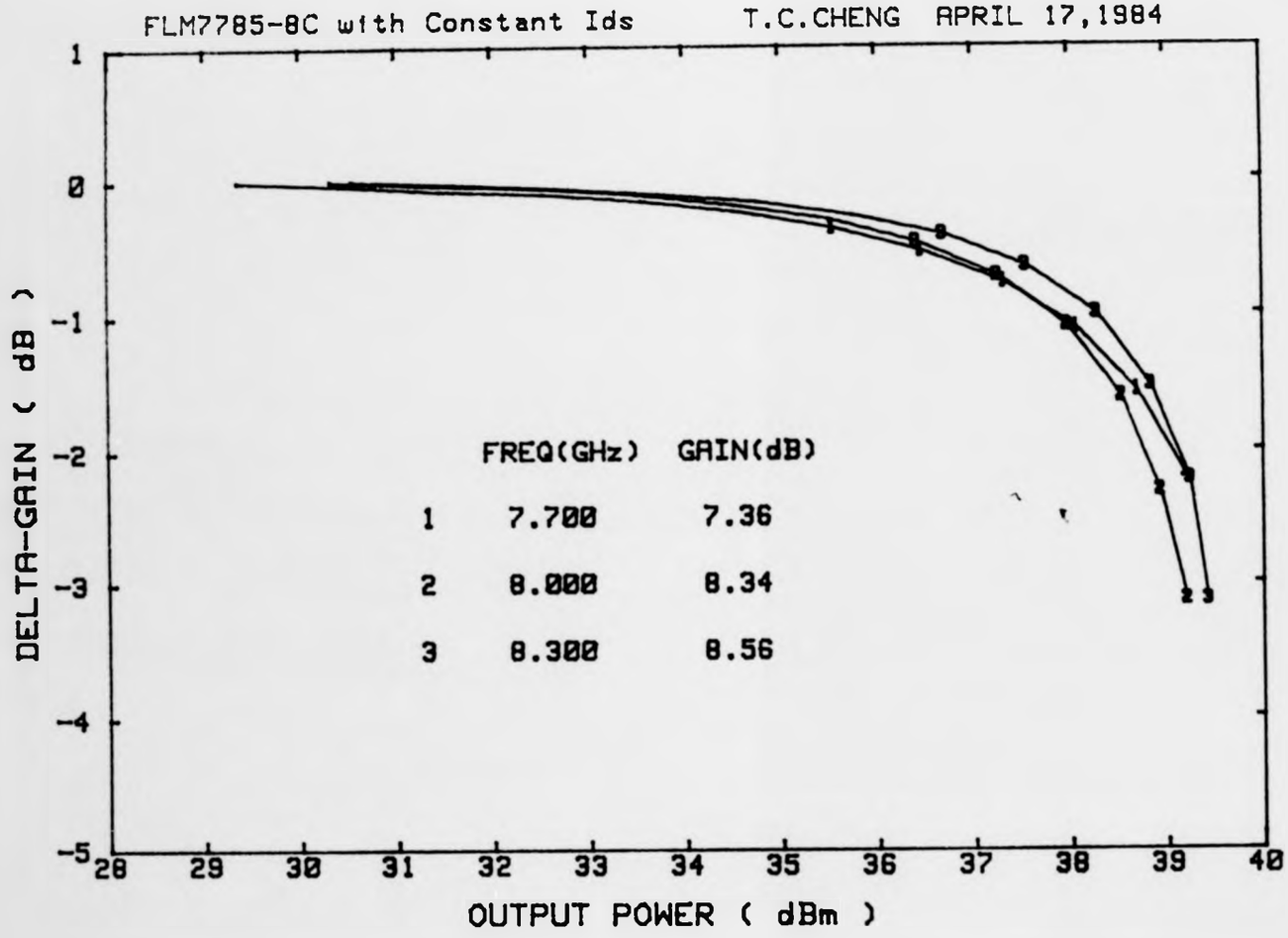


FIGURE 2.7.6 DELTA-PHASE v.s. OUTPUT POWER

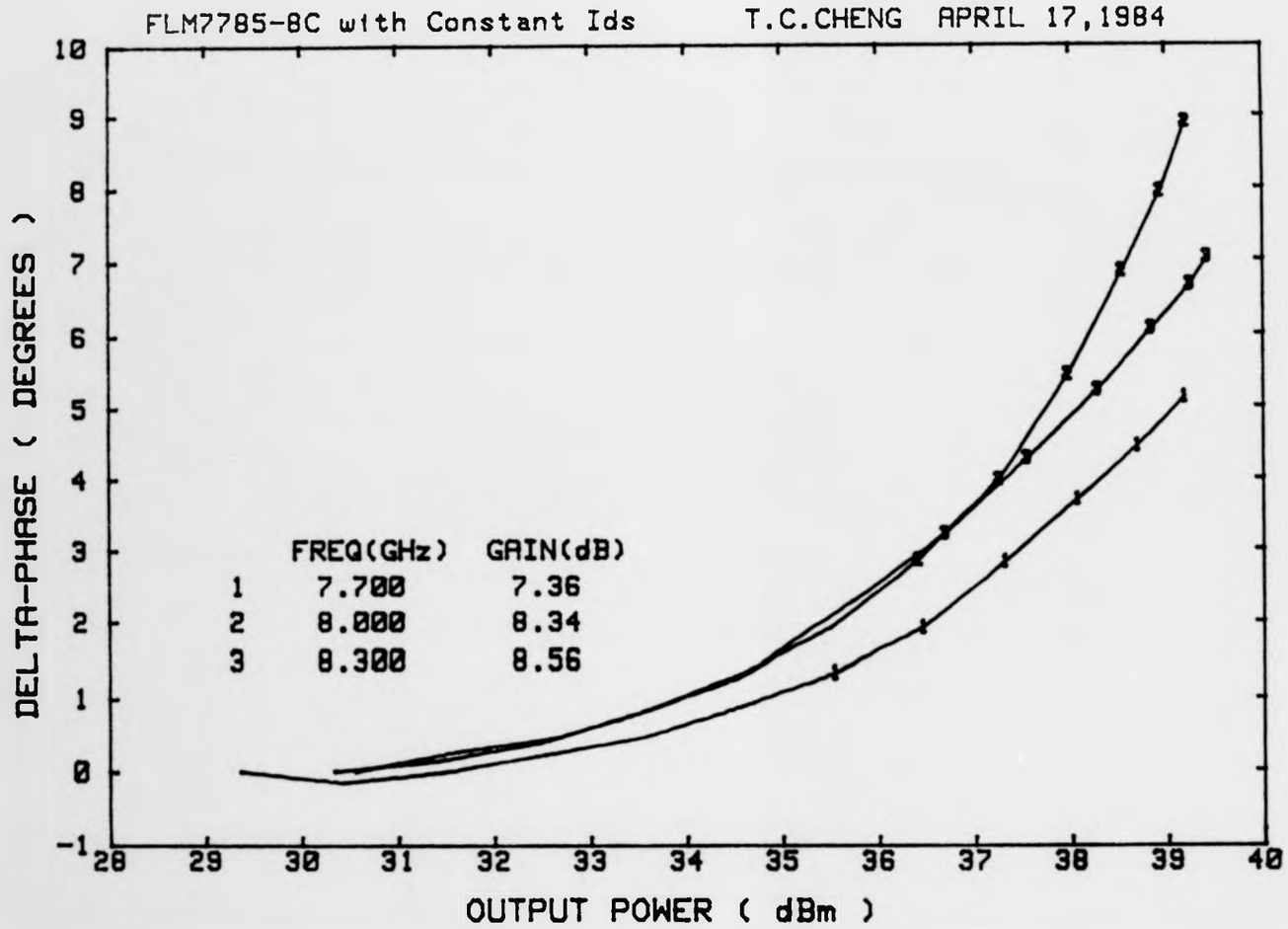


FIGURE 2.7.7 DELTA-GAIN v.s. OUTPUT POWER

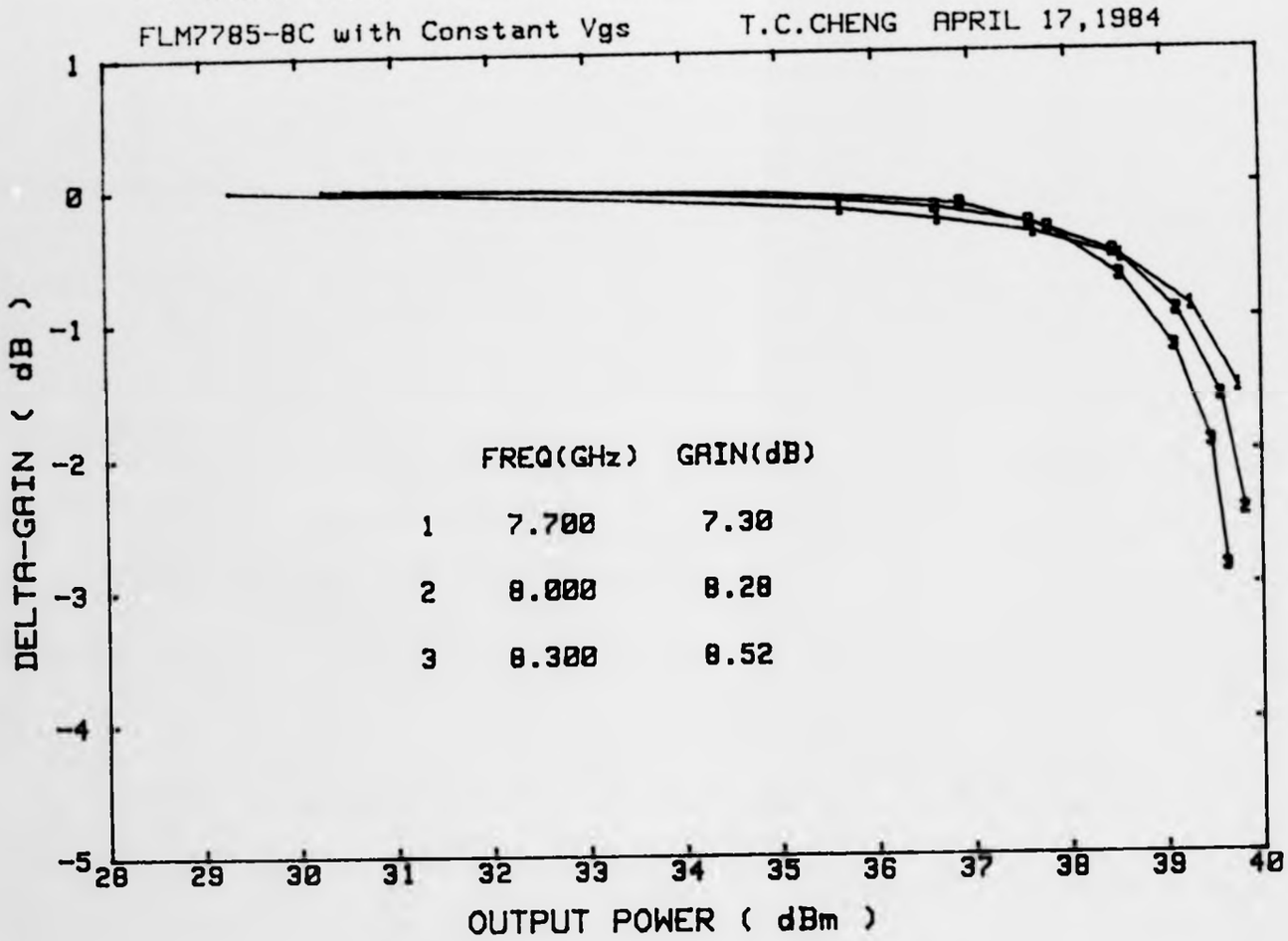


FIGURE 2.7.8 DELTA-PHASE v.s. OUTPUT POWER

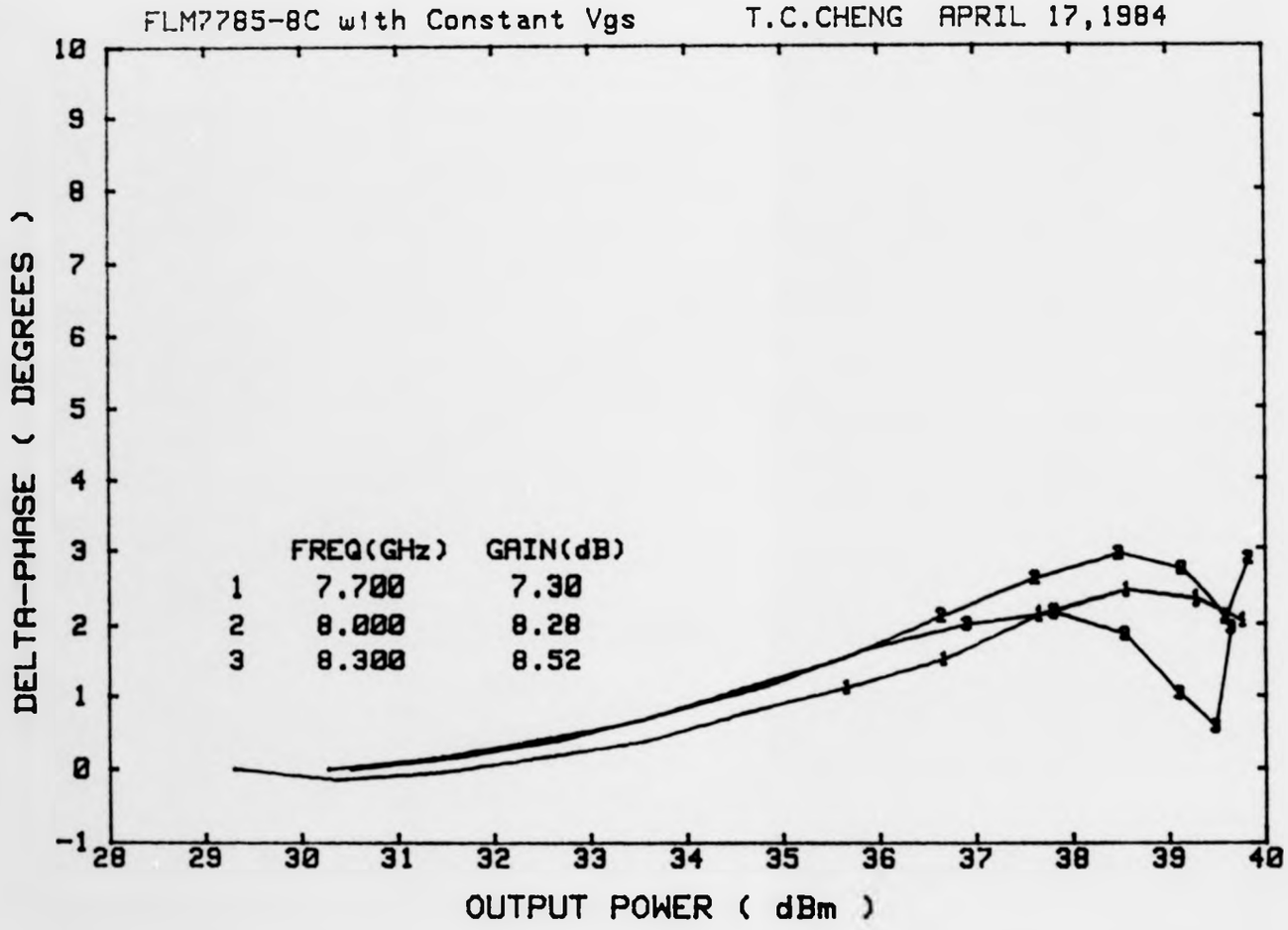


FIGURE 2.7.9 OUTPUT POWER v.s. INPUT POWER

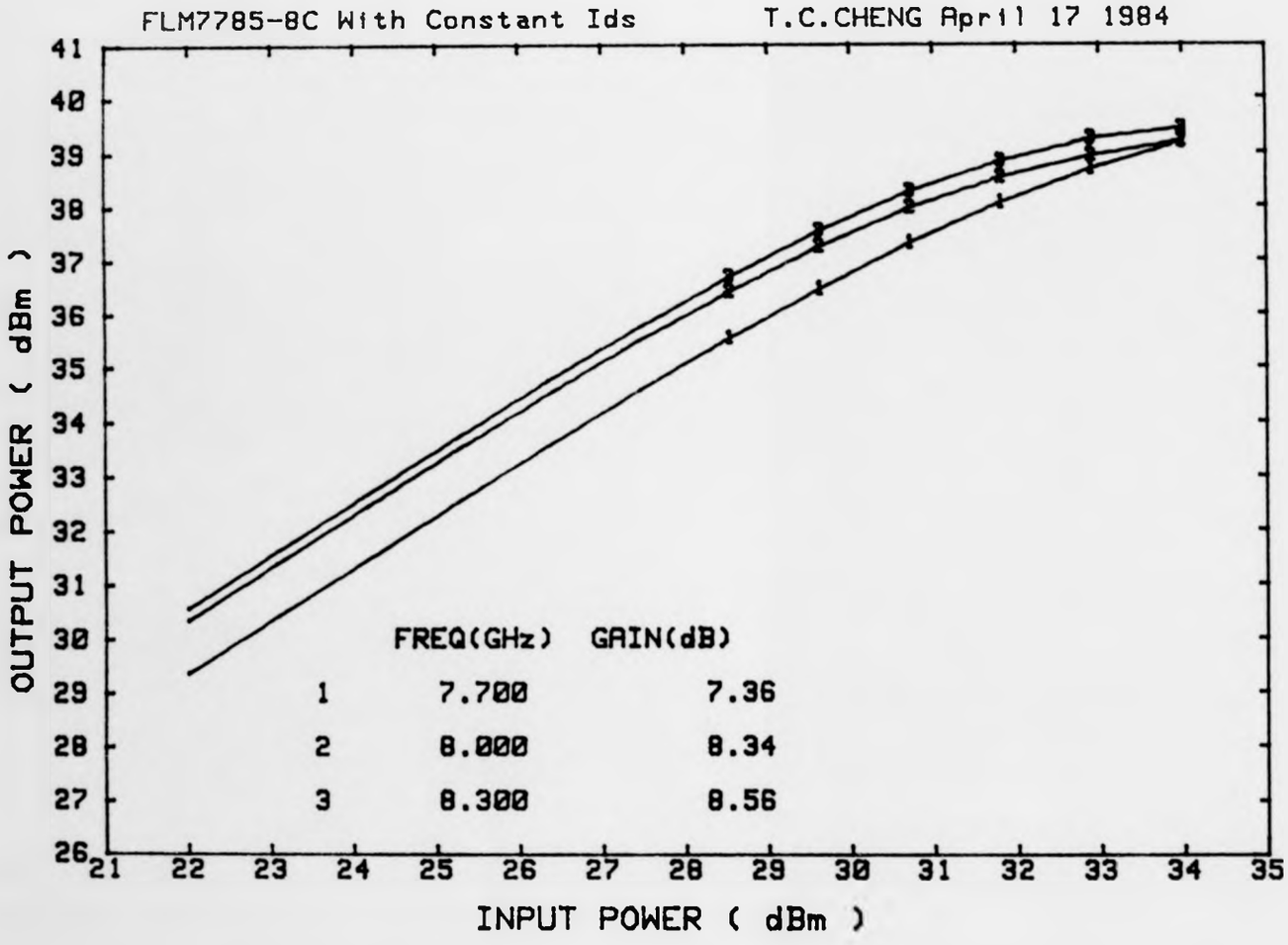
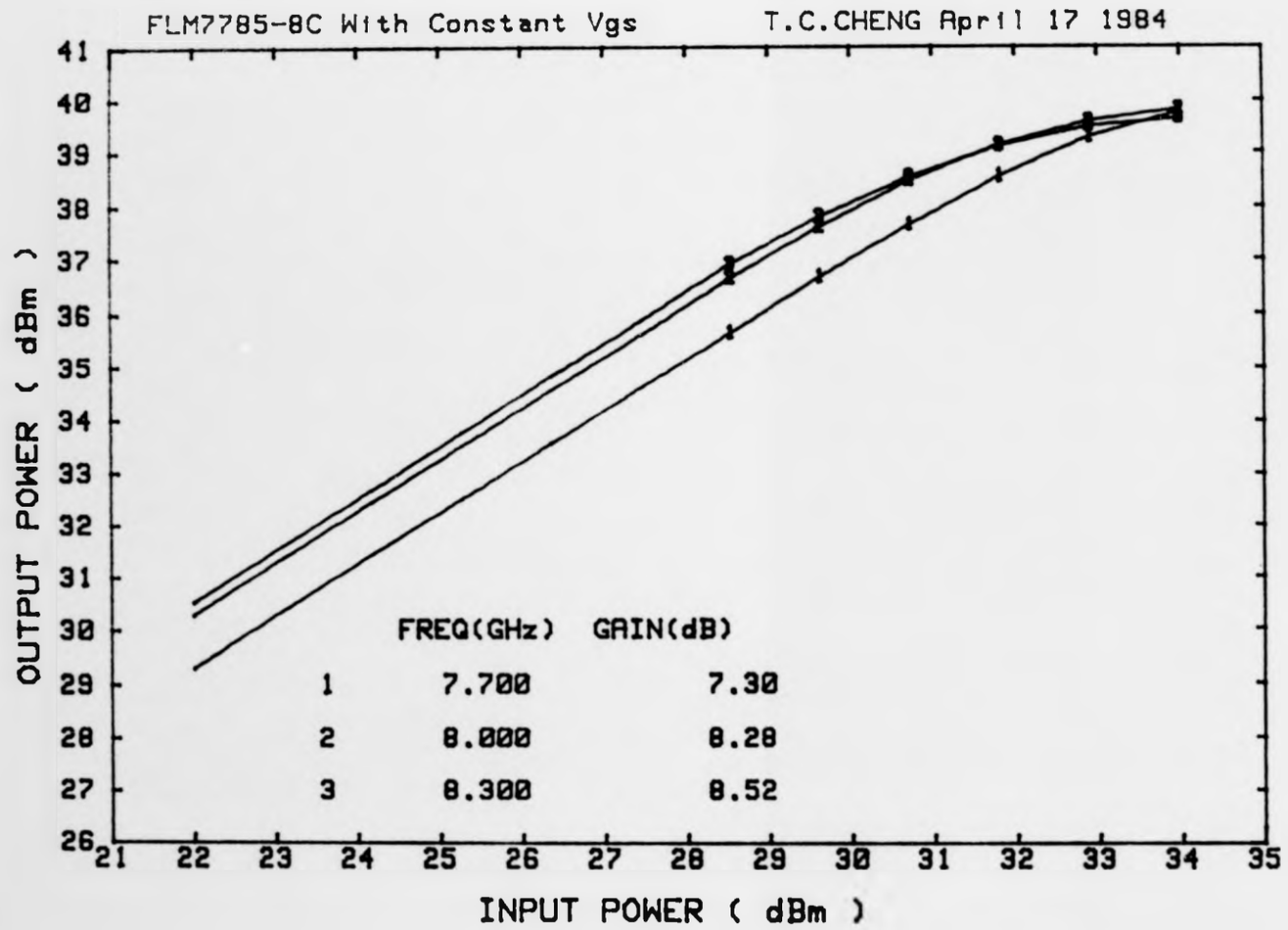


FIGURE 2.7.10 OUTPUT POWER v.s. INPUT POWER



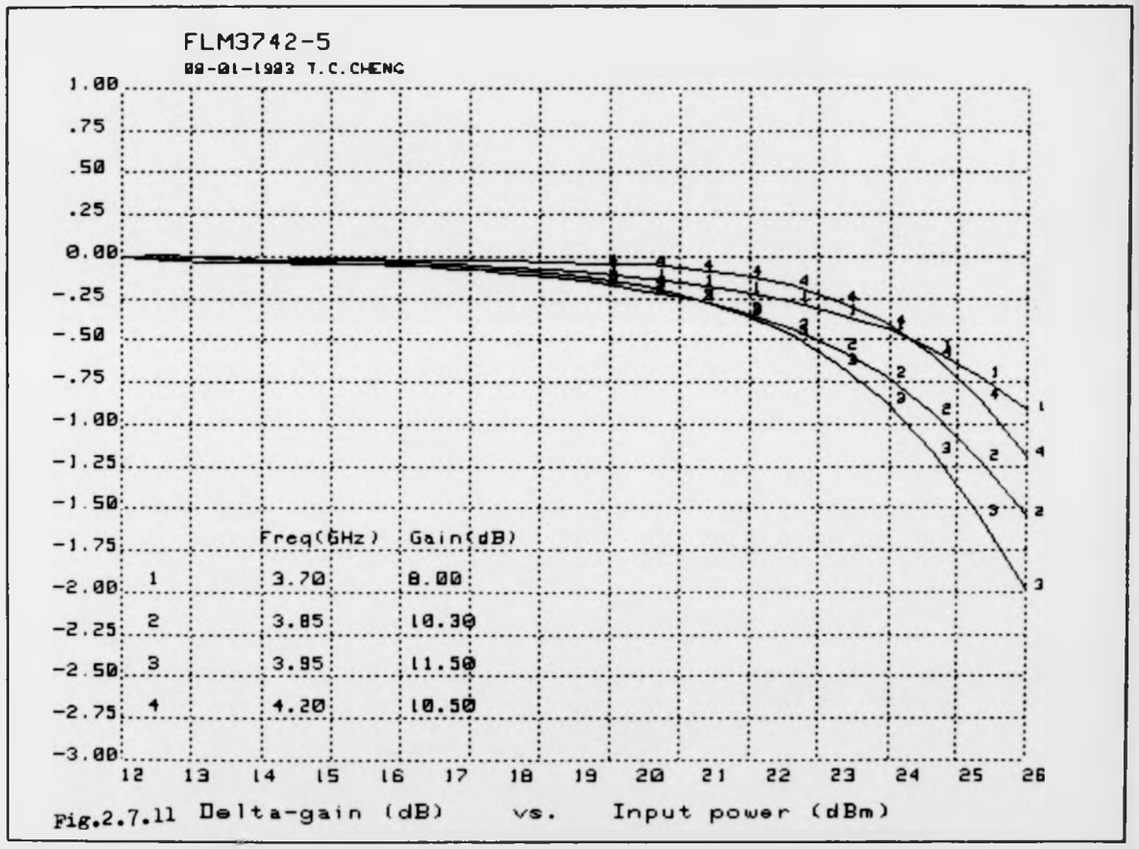


Fig.2.7.11 Delta-gain (dB) vs. Input power (dBm)

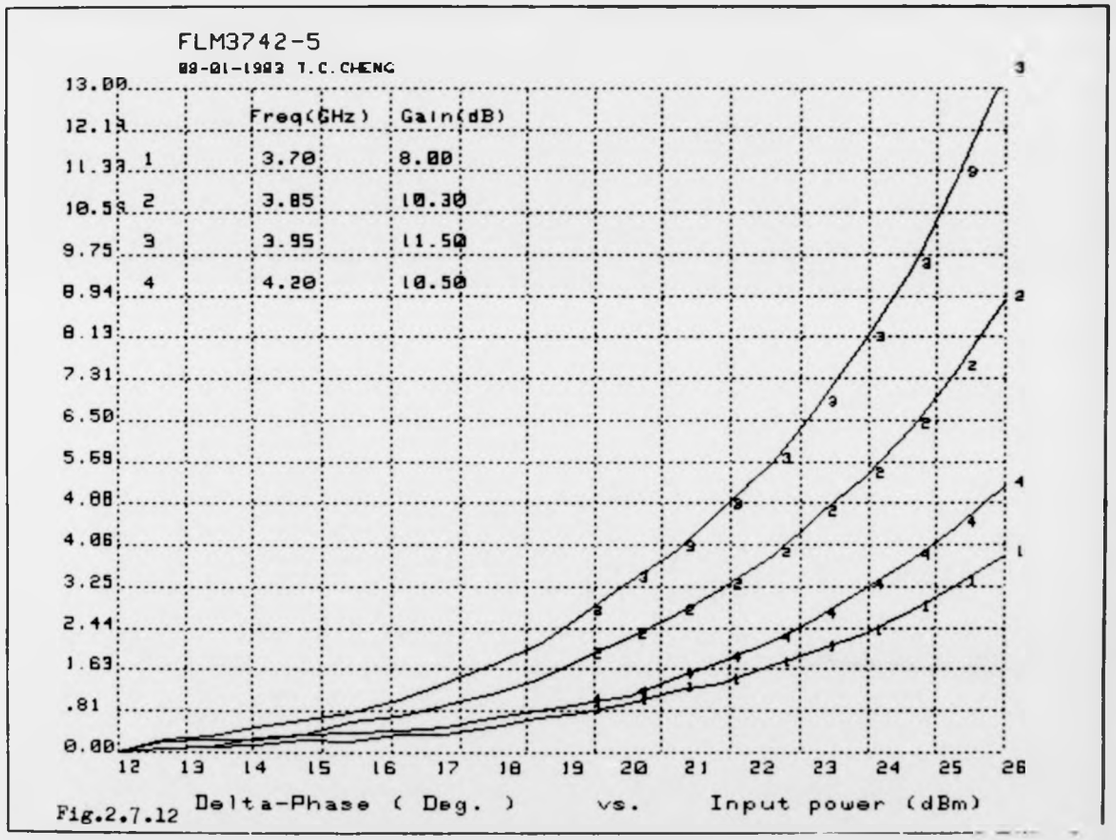

FLM3742-5
09-01-1993 T.C.CHENG
Freq(GHz) Gain(dB)
1 3.70 8.00
2 3.85 10.30
3 3.95 11.50
4 4.20 10.50
13.00
12.19
11.38
10.56
9.75
8.94
8.13
7.31
6.50
5.69
4.88
4.06
3.25
2.44
1.63
.81
0.00
12 13 14 15 16 17 18 19 20 21 22 23 24 25 26
Delta-Phase (Deg.) vs. Input power (dBm)

Fig.2.7.12

2.8 APPLICATION

2.8.1 SIMPLE BIASING CIRCUIT GIVES GaAs FET AMPLIFIER LESS DISTORTION AT HIGH RF POWER LEVEL

It has been proven by experiment that using a simple constant gate voltage biasing circuit as shown in Figure 2.8.1.1 makes a lot of difference to a GaAs FET Amplifier as far as its linearity is concerned, especially the AM to PM conversion factor, which can be improved as much as 6° at 2 dB compression in gain with 39.83 $\overset{dBm}{A}$ output power level at 8 GHz for Fujitsu FLM7785-8c devices, compared with using a constant drain current bias network, shown in Figure 2.5.3.

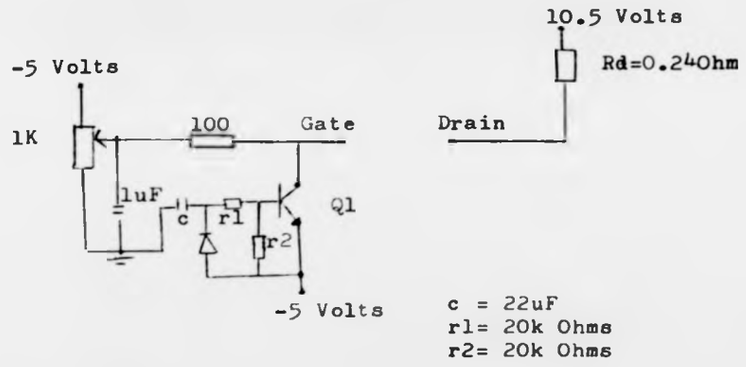
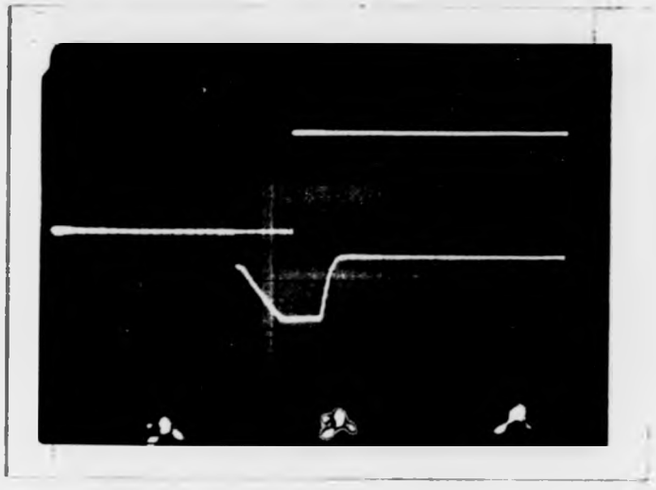


Figure 2.8.1.1 Constant Gate voltage biasing network for high power GaAs FET Devices.

The NPN bipolar transistor Q1 is used for the same purpose as in Figure 2.5.3. i.e., it works as an instant switch, and has been mentioned in Section 2.5.3. The transient response is shown in Figure 2.8.1.2.



Vertical : 5 volt per Division for drain voltage
2.5 volt per Division for gate voltage
Horizontal : 0.5 second per division

Figure 2.8.1.2 Transient response of the switch upon positive D.C. drain voltage turn on.

As a typical example, a Fujitsu high power device FLM7785-8C has been examined. Using the 'CHENG' program for automatic characterizing the nonlinearity of the GaAs FET device, under similar RF conditions, (such as the jig being used for measurements, RF bias and matching networks),the measurement results are shown in Figures 2.7.1 to 2.7.10 of Section 2.7 for both D.C. biasing networks. The drain sensing resistor Rd 0.4=Ohm is used for quiescent condition at Vds=10.0 Volts and Ids=2.1 Amp.

A comparison between Figure 2.7.4 and Figure 2.7.2 shows that constant gate voltage biasing supply gives the following improvements:

1. delta-gain is reduced up to 0.5 dB.
2. delta-phase is reduced up to 6 degrees.
3. Reverse bias gate current is less than .5mA, due to RF signal drift, whilst in the other case it can go to at worst 2.79 mA absolute, which is very damaging to the device life time in the long run.
4. Although the Drain current including RF drift current can increase up to 2.66 Amp., which is 560 mA more then it was in the quiescent condition, the total D.C. power dissipation remains below the power consumed in the quiescent condition.

2.8.2 Pictorical explanation for the measurement results

A typical plot of the Ids vs. Vds d.c. characteristic for the high power GaAs FET device is shown in Figure 2.8.2.1. A simulated curve for a FLM7785-8c device is drawn in quadrant 1 of Figure 2.8.2.2. and an Ids vs. Vgs curve is shown in quadrant 2. In quadrant 3 simulated RF input signals are represented. Input RF signal from quadrant 3 are projected via the Ids-Vgs curve in quadrant 2 into quadrant 1, where the output signal swings along side the dynamic load line L1 passing through the quiescent operating point (10.0 Volt, 2.1 Amp.).

In the case where a constant gate voltage biasing supply is used, the RF signal response superposition with the quiescent point of the GaAs FET device can be illustrated as shown in Figure 2.8.2.2.

The linear output signal D1 corresponds to the small signal S1 applied at the gate of the device. For a large input signal S2, the shape of the signal has been cutoff in both directions, hence a gate current due to RF drift is introduced, the net contribution to the gate current being equal to the RMS subtraction between forward and reverse directions. These are about even for a constant gate voltage supply. For high power operation, one normally sets Ids equal to half of Idss, therefore in the output signal D2 the positive RF drift is greater than the negative one, i.e. the device tends to go more into saturation than pinchoff. In the case of a constant Ids biasing network being chosen, in order to keep the drain current constant when over driven at RF, the effective Vgs is shifted towards the negative; therefore reverse gate current is introduced more and more into the device, as shown in Figure 2.8.2.3.

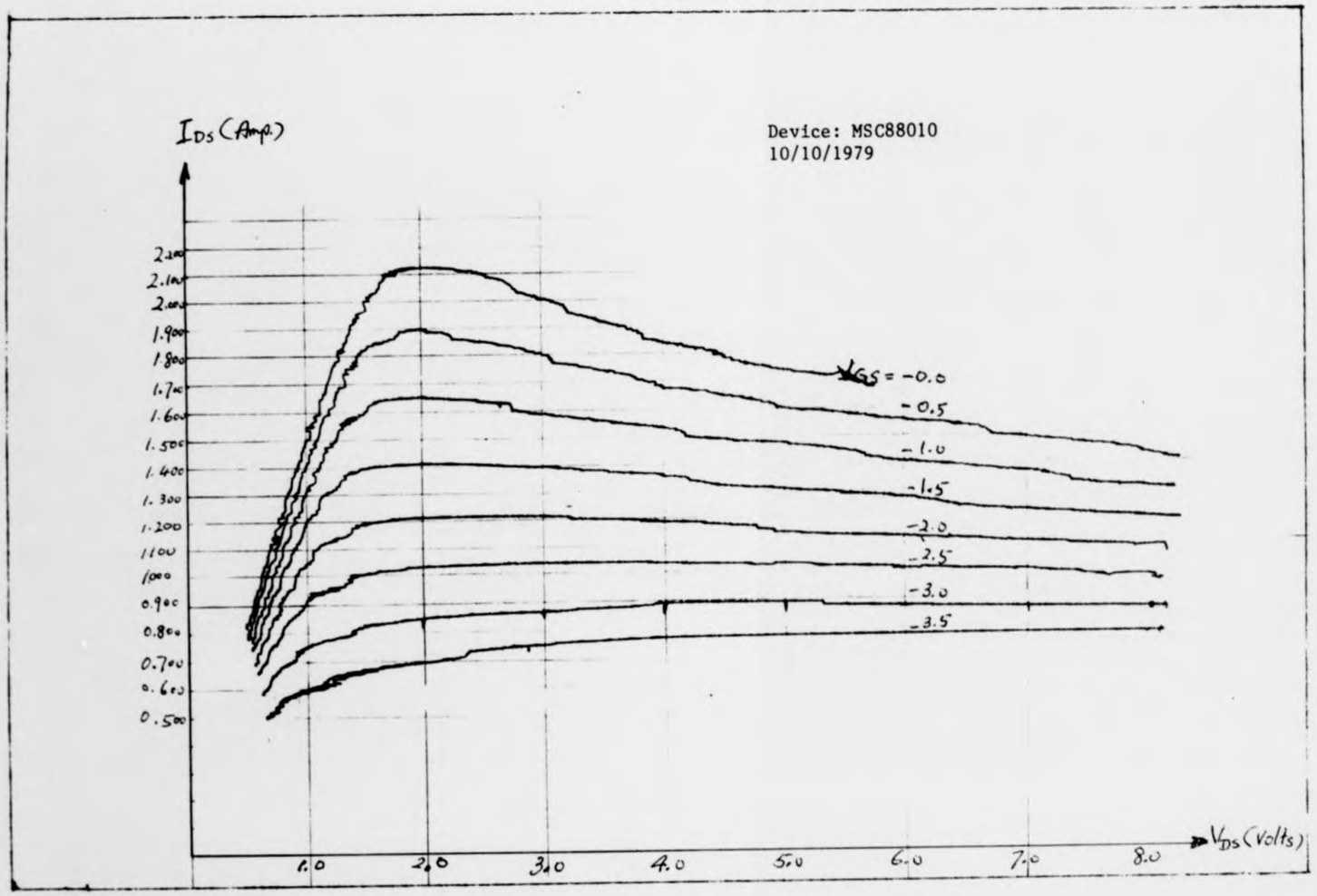


Figure 2.8.2.1 : Measured Static Ids vs. Vds Characteristics for a Power GaAs FET

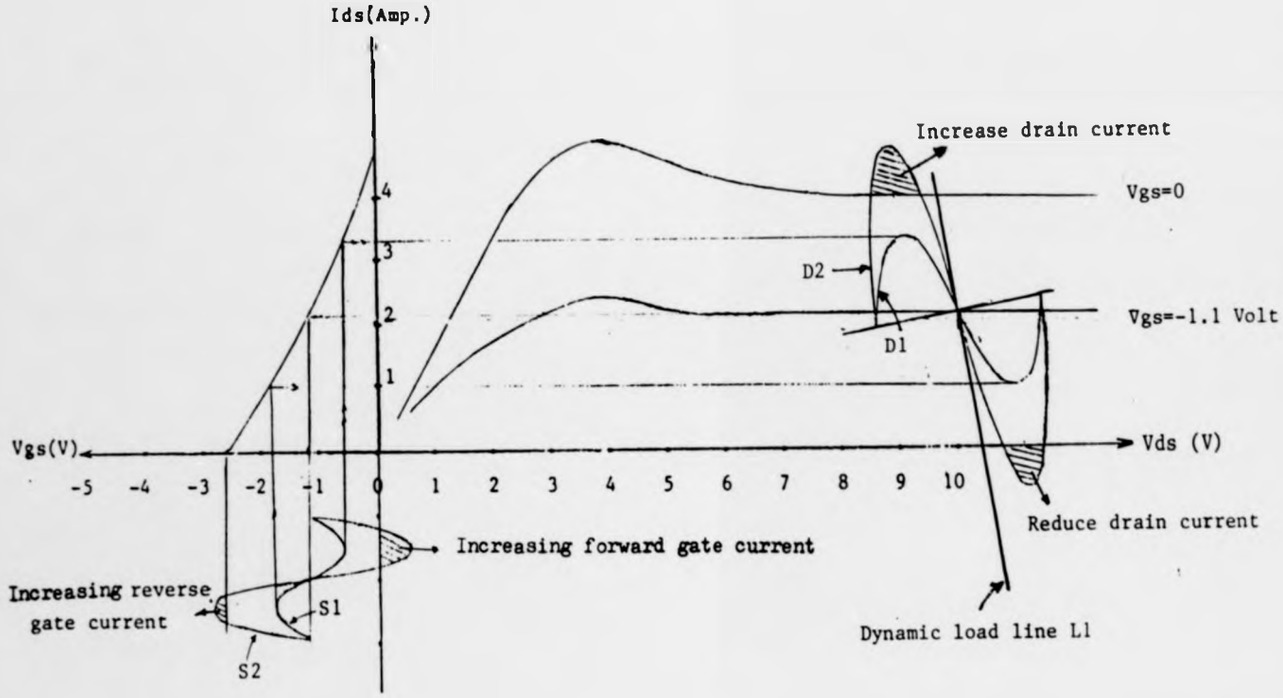


Figure 2.8.2.2 Pictorical illustration of RF signal with constant Vgs biasing network

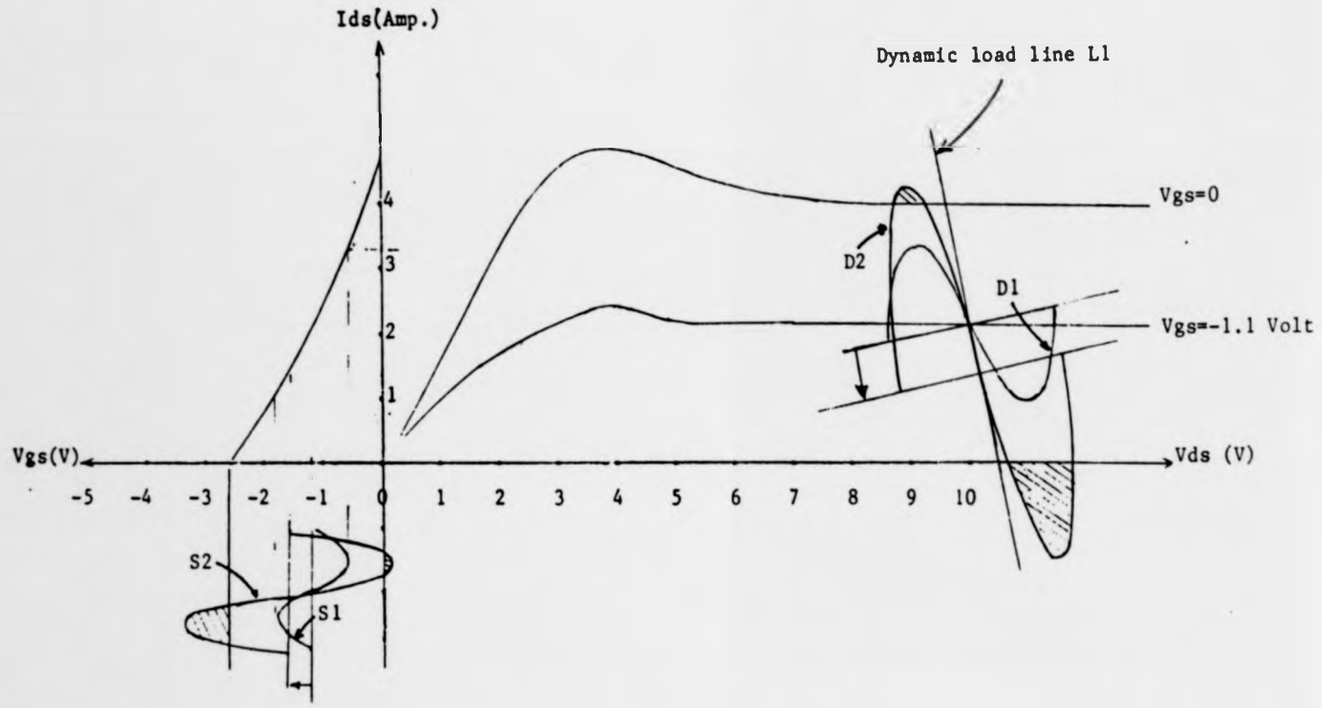


Figure 2.8.2.3 Pictorical illustration of RF signal with constant drain current biasing network

2.9. REFERENCES

1. Ahmed, M.J. "Swept Frequency AM to PM conversion measurement," Microwave Journal, Vol.20, No.20, (Dec. 1977),pp.58-59.
2. Garrison, G.J.,"Intermodulation Distortion in Frequency-Division-Multiplex FM Systems-A Tutorial Summary," IEEE Trans. on Communication Technology, Vol. COM-16, April, 1968, pp.289-303.
3. Sproul, P.T. and H.D. Griffiths, "The TH Broadband Radio Transmitter and Receiver, "Bell System Technical Journal, Vol.XL, Nov, 1961, pp. 1542-1547.
4. Cheng, T.C. "Introduction to Microwave Software Packages:
   (1) Stability of GaAs FET Devices
   (2) Delta-gain and delta-Phase Measurements."
   Seminar on 22nd July, 1983 in Dept. of Radio Design, A & R Transmission Div., Northern Telecom, Montreal, Canada.
5. HP Application Note 117-1: "Microwave network Analyzer Applications," pp.3-6 to 3-7.
6. Lane, R.Q. "Bias Regulator For Power GaAs FET Testing," California Eastern Laboratories, Application Note. 1978.
7. Hp 59313A Analog to Digital Converter," Operating and Service Manual," p.2-2.

2.10 PROGRAM LISTING

```
10     !         PROGRAM NAME : CHENG
20     !         AUTHOR   :  T.C.CHENG
30     !         DELTA GAIN AND DELTA PHASE MEASUREMENTS ( FOR HP9816 COMPUTER )
40     !THIS PROGRAM HAS BEEN DEVELOPED ON 11th Nov.,1982 USING HP9845 COMPUERTER
50     !
60     !           DECLARATION
70     !
80        OPTION BASE 1
90        DIM Pin(10,20),Freq(10),P(10,20)
100       DIM P0(10),G(10)
110       DIM P1(10),X(10,20),Y(10,20)
120       DIM P9(10),Q9(10)
130       DIM F0(20),Pout(10,20),A0(20)
140       DIM A3(10,20),F3(10,20)
150       DIM A4(10,20),F4(10,20)
160       DIM De_gain(10,20),De_phase(10,20)
170       DIM Igs0(10,20),Ids0(10,20),Vgs0(10,20),Vds0(10,20),Ids(20),Vds(20)
180       DIM Igs(20),Vgs(20),Tg(10),Tg12(10),Tg13(10),Tg0(10)
190       DIM Igsf(10,20),Vgsf(10,20),Idsf(10,20),Vdsf(10,20)
200       DIM A1(10,20),F1(10,20),Eff(10,20)
210       DIM Text1$[100],Text2$[80],Labelx1$[80],Labelt$[80],Labelx2$[80]
220       DIM Data_file$[20],Labely$[100],Ques1$[80],Ques2$[80],Ques3$[80]
230       DIM Title$[100],Ques4$[80],Ques5$[80],Ques6$[80],Ques7$[80]
240       DIM Name_date$[100]
250       DIM Ans$[3],Off$[1],Dev$[20],Ser$[8],Date$[20],Ids$[20],Vds$[20]
260       Ans$="N"
270  Image0:IMAGE  "PL",DDD.DD,"DM"
280  Image1:IMAGE MDD.DD,2X,MDD.DD,2X,MDD.DD,2X,MDD.DD,2X,MDDDD.DD,2X,MDDDD.DD,2X
,MDDDD.DD,2X,MDD.DD,2X,MDD.DD
290  Image2:IMAGE  4(6D)
300  Image3:IMAGE  "H",D,"AJ"
310  Image4:IMAGE  #,W
320  Image5:IMAGE 5X,MDD.DDD,8X,MDD.DD
330  Image6:IMAGE 2X,MD.4X,MDD.DDD.8X,MDD.DD
340  !
350  !       INTERFACE & SET KEYS
360  !
370       ABORT 7
380       CLEAR 7
390       LOCAL 7
400       REMOTE 7
410       S0=719
420       Ao=710
430       M12=712
440       M13=713
450       Off$="0"
460       Labelx1$=" OUTPUT POWER ( dBm )"
470       Labelx2$=" INPUT POWER ( dBm )"
480       Ques1$="MINIMUM INPUT POWER LEVEL (dBm) = "
490       Ques2$="MAXIMUM INPUT POWER LEVEL (dBm) = "
500       Ques3$="MAXIMUM OUTPUT POWER LEVEL (dBm) = "
```

```
510       Ques4$="MINIMUM OUTPUT POWER LEVEL (dBm) = "
520       GINIT
530       GRAPHICS ON
540       X_gdu_max=100*MAX(1,RATIO)!
550       Y_gdu_max=100*MAX(1,1/RATIO)!
560       ON ERROR GOTO Terror
570 Setkeys:OUTPUT SO;"RFO"
580       Mea_flag=0
590       PRINT " "
600       ON KEY 0 LABEL "CALIBRATION" GOTO Calibration
610       ON KEY 1 LABEL "MEASUREMENT" GOTO Measurement
620       ON KEY 2 LABEL "GET CAL-DATA TAPE" GOTO Get_cal_data
630       ON KEY 3 LABEL "GET MEAS-DATA TAPE" GOTO Get_meas_data
640       ON KEY 4 LABEL "STORE DATA" GOTO Store
650       ON KEY 5 LABEL "A/D TEST" GOTO Test
660       ON KEY 6 LABEL "TABULATE" GOTO Tabulation
670       ON KEY 7 LABEL "Pt-DELTA-GAIN" GOTO Pt_del_gain
680       ON KEY 8 LABEL "Pt-DELTA-PHASE" GOTO Pt_del_phase
690       ON KEY 9 LABEL "Pt-Pin-Pout" GOTO Pt_pin_pout
700       PRINT " "
710       PRINT " READY"
720 Dummy:GOTO Dummy
730 Terror:PRINT " SOMETHING WRONG !"
740       GOTO Setkeys
750 Error:PRINT " "
760       PRINT " PHASE OFFSET HAS DONE!"
770       BEEP
780       IF Off$="O" THEN GOTO Change
790       Off$="O"
800       GOTO No_change
810 Change:Off$="N"
820 No_change:OUTPUT 710;Off$
830       PRINT "TAKING DATA"
840       GOTO Noerror
850 !
860 !       CALIBRATION
870 !
880 Calibration:PRINT "Delta-GAIN & Delta-PHASE measurement "
890       PRINT " "
900       PRINT " Number OF FREQ to be MEASURED (Max 10)=";
910       Freq_number=3 ! Default number
920    INPUT Freq_number
930       PRINT Freq_number
940       PRINT " "
950       PRINT "NUMBER OF MEASUREMENT (# of repeat for each step (10 max)="
960       C8accuracy=7   ! Default number
970    INPUT C8accuracy
980       PRINT C8accuracy
990       PRINT " "
1000      PRINT " NUMBER OF TEST POINTS (# OF STEPS FOR EACH FREQ CW (20MAX)=";
```

```
1010      Cw_step_number=12 ! Default number
1020 INPUT Cw_step_number
1030      PRINT Cw_step_number
1040      PRINT " "
1050      PRINT " ACTUAL START POWER LEVEL (dBm)= ";
1060 INPUT P1_ac_start
1070      PRINT P1_ac_start
1080      PRINT " ACTUAL STOP POWER LEVEL (dBm)= ";
1090 INPUT P1_ac_stop
1100      PRINT P1_ac_stop
1110      PRINT " "
1120      PRINT "PRINTER NUMBER (PRINTER=701 or CRT=1)=";
1130      Printer=1 ! Default number
1140 INPUT Printer
1150      PRINT Printer
1160  !
1170  !      TAKING FREQ VALUE
1180  !
1190  !   SET DEFAULT VALUES
1200  !
1210      Freq(1)=7.7
1220      Freq(2)=8.0
1230      Freq(3)=8.3
1240      P0(1)=7.5
1250      P0(2)=9.7
1260      P0(3)=8.0
1270      P1(1)=17.4
1280      P1(2)=19.8
1290      P1(3)=18.3
1300      FOR M=1 TO Freq_number
1310                PRINT " FREQ (GHz) =           ";
1320 INPUT Freq(M)
1330                PRINT Freq(M)
1340                PRINT " "
1350  !
1360  !       TAKING INPUT POWER LEVELS
1370  !
1380                PRINT "START POWER SWEEP (dBm) =";
1390 INPUT P0(M)
1400                PRINT P0(M)
1410                PRINT " "
1420                PRINT "STOP POWER SWEEP (dBm)=";
1430 INPUT P1(M)
1440                PRINT P1(M)
1450                PRINT " "
1460  !
1470  !       SET POWER STEP LEVELS
1480  !
1490                Q9(M)=(P1_ac_stop-P1_ac_start)/(Cw_step_number-1)
1500                FOR K=1 TO Cw_step_number
```

```
1510                        Pin(M,K)=P1_ac_start+Q9(M)*(K-1)
1520                NEXT K
1530                P9(M)=(P1(M)-P0(M))/(Cw_step_number-1)
1540                FOR I=1 TO Cw_step_number
1550                        P(M,I)=P0(M)+P9(M)*(I-1)
1560                NEXT I
1570        NEXT M
1580        FOR M=1 TO Freq_number
1590                GOSUB Gain_sub
1600                Tg(M)=Tg0(M)
1610        NEXT M
1620    !
1630    !       TAKING MEASUREMENT DATA
1640    !
1650        FOR M=1 TO Freq_number
1660                GOSUB Switch_cw_sub
1670                FOR K=1 TO Cw_step_number
1680                        A3(M,K)=A0(K)
1690                        F3(M,K)=F0(K)
1700                NEXT K
1710        NEXT M
1720        OUTPUT S0;"RF0"
1730        PRINT "STORE CALIBRATION DATA?(Y/N)";
1740        INPUT Ans$
1750        PRINT Ans$
1760        IF Ans$="Y" THEN GOSUB Store_data
1770        GOTO Setkeys
1780 !
1790 Measurement:!
1800 !
1810        Flag_data=1
1820        PRINT "ALL FREQ ? YES=1 NO=0";
1830        INPUT Freq_all
1840        PRINT Freq_all
1850        PRINT " "
1860        PRINT "NUMBER OF MEASUREMENT 10 MAX";
1870                INPUT C8accuracy
1880        PRINT C8accuracy
1890        PRINT " "
1900        PRINT "FREQ (GHz)";"    GAIN(dB)"
1910        FOR M=1 TO Freq_number
1920                GOSUB Gain_sub
1930                G(M)=Tg0(M)-Tg(M)
1940                PRINT Freq(M);"     ";G(M)
1950        NEXT M
1960        PRINT " "
1970        IF Freq_all=1 THEN GOTO All
1980 Back: PRINT "NUMBER ";"        FREQ(GHz)"
1990        FOR I=1 TO Freq_number
2000                PRINT I;"            ";Freq(I)
```

```
2010      NEXT I
2020      PRINT " "
2030      PRINT "NUMBER  = ";
2040      INPUT M
2050      PRINT M
2060      PRINT " "
2070      IF M>Freq_number THEN GOTO New_device
2080      GOSUB Calculate1
2090      GOSUB Calculate2
2100      GOSUB Print
2110      GOTO Back
2120 All:FOR M=1 TO Freq_number
2130      GOSUB Calculate1
2140      NEXT M
2150      OUTPUT S0;"RF0"
2160 New_device:FOR M=1 TO Freq_number
2170      GOSUB Calculate2
2180      NEXT M
2190      PRINT "STORE MEASUREMENT DATA ?Y/N";
2200      INPUT Ans$
2210      PRINT Ans$
2220      IF Ans$="Y" THEN GOSUB Store_data
2230      GOTO Setkeys
2240 !
2250 Gain_sub:OUTPUT S0;"CW";Freq(M);"GZ"
2260 !
2270      OUTPUT S0 USING Image0;P0(M)
2280      OUTPUT S0;"RF1"
2290      PRINT " MEASURE POWER METER !"
2300      PAUSE
2310      ENTER M12;Tg12(M)
2320      ENTER M13;Tg13(M)
2330      Tg0(M)=Tg12(M)-Tg13(M)
2340      PRINT Freq(M);" ";Tg0(M)
2350      RETURN
2360 !
2370 Switch_cw_sub:OUTPUT S0;"CW";Freq(M);"GZ"
2380      OUTPUT S0 USING Image0;P0(M)
2390      PRINT "TAKING DATA ... "
2400      FOR J=1 TO C8accuracy
2410 Noerror:       OUTPUT S0 USING Image0;P(M,1)
2420                FOR K=1 TO Cw_step_number
2430                          OUTPUT S0 USING Image0;P(M,K)
2440                          GOSUB Read_a_d
2450                          IF ABS(D(2))>1000 THEN GOTO Error
2460                          F1(J,K)=D(2)    ! Ao=710 Ch.2 Phase
2470                          A1(J,K)=D(3)    ! Ao=710 Ch.3 Amplitude
2480                          Igs0(J,K)=Dd(1)-(-3)! Ao=706 Ch.1 Igs (2.5V)
2490                          Ids0(J,K)=Dd(2)-(+1)! Ao=706 Ch.2 Ids (1.0V)
2500                          Vgs0(J,K)=Dd(3)-(-0)! Ao=706 Ch.3 Vgs (5.0V)
```

```
2510                        Vds0(J,K)=Dd(4)-(-9)! Ao=706 Ch.4 Vds (10.V)
2520                NEXT K
2530      NEXT J
2540      OUTPUT S0 USING Image0;P0(M)
2550 !
2560 !            OFFSET DATA TO ZEROS
2570 !
2580      FOR J=1 TO C8accuracy
2590                FOR K=2 TO Cw_step_number
2600                        A1(J,K)=A1(J,K)-A1(J,1)
2610                        F1(J,K)=F1(J,K)-F1(J,1)
2620                NEXT K
2630                A1(J,1)=0
2640                F1(J,1)=0
2650      NEXT J
2660  !
2670  !         INITIAL ZERO SUM
2680  !
2690      FOR K=1 TO Cw_step_number
2700                A0(K)=0
2710                F0(K)=0
2720      NEXT K
2730           !TAKING AVERAGE
2740      FOR K=2 TO Cw_step_number
2750                FOR J=1 TO C8accuracy
2760                        A0(K)=A0(K)+A1(J,K)
2770                        F0(K)=F0(K)+F1(J,K)
2780                NEXT J
2790                A0(K)=A0(K)/C8accuracy
2800                F0(K)=F0(K)/C8accuracy
2810      NEXT K
2820      RETURN
2830 Calculate1:!
2840                GOSUB Switch_cw_sub
2850                !INITIAL BIAS VALUE
2860                FOR K=1 TO Cw_step_number
2870                Igs(K)=0
2880                Ids(K)=0
2890                Vgs(K)=0
2900                Vds(K)=0
2910                NEXT K
2920                '
2930                FOR K=1 TO Cw_step_number
2940                   FOR J=1 TO C8accuracy
2950                   Igs(K)=Igs0(J,K)+Igs(K)
2960                   Ids(K)=Ids0(J,K)+Ids(K)
2970                   Vgs(K)=Vgs0(J,K)+Vgs(K)
2980                   Vds(K)=Vds0(J,K)+Vds(K)
2990                   NEXT J
3000                        A4(M,K)=A0(K)
```

```
3010                        F4(M,K)=F0(K)
3020       Igsf(M,K)=2500*Igs(K)/(C8accuracy*300)!R_gate=300 ohms(2.5:1000)
3030       Idsf(M,K)=-Ids(K)/(C8accuracy*.25)! R_drain =0.25 ohm  (1.0:1000)
3040       Vgsf(M,K)=-5*Vgs(K)/(C8accuracy)!    (5.0:1000)
3050       Vdsf(M,K)=Vds(K)/(C8accuracy*100) ! (10.:1000)
3060                NEXT K
3070  RETURN
3080 Calculate2:!
3090                FOR J=1 TO Cw_step_number
3100                        De_gain(M,J)=(A4(M,J)-A3(M,J))/50
3110                        De_phase(M,J)=(F4(M,J)-F3(M,J))/10
3120                        Pout(M,J)=De_gain(M,J)+G(M)+Pin(M,J)
3130                NEXT J
3140 RETURN
3150 !
3160 Tabulation:!
3170 !
3180     PRINT " TITLE = ";
3190     INPUT Title$
3200     PRINT Title$
3210     PRINT "PRINTER NUMBER (PRINTER =701 OR CRT=1 )";
3220     Printer=1
3230     INPUT Printer
3240     PRINT Printer
3250     PRINTER IS Printer
3260     PRINT Title$
3270     FOR M=1 TO Freq_number
3280                GOSUB Print
3290     NEXT M
3300     PRINTER IS 1
3310     GOTO Setkeys
3320 !
3330 !          PRINT RESULT
3340 !
3350 Print:PRINT TIME$(TIMEDATE)
3360     PRINT "FREQ (GHz) = ";Freq(M);" GAIN (dBm) = ";G(M)
3370     PRINT " "
3380 PRINT " INPUT   OUTPUT Del-Gain Del-Phase  Igs       Vgs        Ids       Vds
    Eff."
3390     PRINT " (dBm)    (dBm)    (dB)      (dgrees)  (ua)      (mv)       (ma)
(V)      (%)"
3400     PRINT " "
3410     FOR J=1 TO Cw_step_number
3420     ! ADDED EFFECIENCY = (Pout-Pin)/(Pdc+Pin)
3430     Poutput=10^(Pout(M,J)/10)
3440     Pinput=10^(Pin(M,J)/10)
3450     Eff(M,J)=100*(Poutput-Pinput)/(Vdsf(M,J)*Idsf(M,J)+Pinput)
3460   PRINT USING Image1;Pin(M,J);Pout(M,J);De_gain(M,J);De_phase(M,J);Igsf(M,J
);Vgsf(M,J);Idsf(M,J);Vdsf(M,J),Eff(M,J)
3470     NEXT J
3480     PRINT " "
3490     RETURN
3500 !
```

```
3510 Store: !
3520 !
3530      PRINT " STORE DATA : CALIBRATION TYPE 0"
3540      PRINT "              MEASUREMENT TYPE 1"
3550      INPUT Flag_data
3560      PRINT Flag_data
3570                    !
3580                    !       STORE MEASUREMENT DATA
3590                    !
3600 Store_data:!
3610      MASS STORAGE IS ":HP82901,700,1"
3620      PRINT "DATA FILE NAME= ";
3630      INPUT Data_file$
3640      PRINT Data_file$
3650      IF Flag_data=1 THEN GOTO Meas_data
3660      CREATE BDAT Data_file$,30
3670      ASSIGN @Path_1 TO Data_file$
3680      OUTPUT @Path_1;A3(*),F3(*),Freq_number,Cw_step_number,Freq(*),P0(*),P(*
),Pin(*),Tg(*),C8accuracy
3690      GOTO Cont
3700 Meas_data:CREATE BDAT Data_file$,60
3710      ASSIGN @Path_1 TO Data_file$
3720      OUTPUT @Path_1;Pin(*),Pout(*),De_gain(*),De_phase(*),Freq(*),Cw_step_nu
mber,G(*),Freq_number,Igsf(*),Vgsf(*),Idsf(*),Vdsf(*)
3730 Cont: !
3740      ASSIGN @Path_1 TO *
3750      MASS STORAGE IS ":HP82901,700,0"
3760      GOTO Setkeys
3770 !
3780 !          GET DATA FROM DISC
3790 !
3800 Get_cal_data:!
3810      MASS STORAGE IS ":HP82901,700,1"
3820      PRINT "CALIBRATION-DATA FILE NAME=  ";
3830      INPUT Data_file$
3840      PRINT Data_file$
3850      ASSIGN @F_1 TO Data_file$
3860      ENTER @F_1;A3(*),F3(*),Freq_number,Cw_step_number,Freq(*),P0(*),P(*),Pi
n(*),Tg(*),C8accuracy
3870      ASSIGN @F_1 TO *
3880      MASS STORAGE IS ":HP82901,700,0"
3890      GOTO Setkeys
3900        !
3910        !       GET MEASUREMENT DATA FROM DISC
3920        !
3930 Get_meas_data:PRINT "MEASURED-DATA FILE NAME=  ";
3940      INPUT Data_file$
3950      PRINT Data_file$
3960      MASS STORAGE IS ":HP82901,700,1"
3970      ASSIGN @F_1 TO Data_file$
3980      ENTER @F_1;Pin(*),Pout(*),De_gain(*),De_phase(*),Freq(*),Cw_step_number
,G(*),Freq_number,Igsf(*),Vgsf(*),Idsf(*),Vdsf(*)
3990      ASSIGN @F_1 TO *
4000      MASS STORAGE IS ":HP82901,700,1"
```

```
4010      GOTO Setkeys
4020 !
4030 !       A/D READ
4040 !
4050 Read_a_d_2:OUTPUT Ao USING Image3;2^(N-1)
4060      ENTER Ao USING Image4;C3
4070      RETURN
4080 Read_a_d:!
4090           Ao=710
4100      FOR N=2 TO 3
4110                OUTPUT Ao USING Image3;2^(N-1)
4120                ENTER Ao USING Image4;D(N)
4130      NEXT N
4140           Ao=706
4150      FOR N=1 TO 4
4160                OUTPUT Ao USING Image3;2^(N-1)
4170                ENTER Ao USING Image4;Dd(N)
4180      NEXT N
4190      PRINT USING Image2;D(2),D(3),Dd(1),Dd(2),Dd(3),Dd(4)
4200      RETURN
4210 Test: !
4220      FOR N=1 TO 4
4230      Ao=710
4240                GOSUB Read_a_d_2
4250                D(N)=C3
4260      Ao=706
4270                GOSUB Read_a_d_2
4280                Dd(N)=C3
4290      NEXT N
4300      PRINT USING Image2;D(1),D(2),D(3),D(4),Dd(1),Dd(2),Dd(3),Dd(4)
4310      GOTO Test
4320 !
4330 Pt_del_gain:!
4340 !
4350      Labely$=" DELTA-GAIN ( dB )"
4360      Text1$=" DELTA-GAIN  v.s. OUTPUT POWER "
4370      Text2$=" DELTA-GAIN  v.s. INPUT POWER "
4380      Label$="DELTA-GAIN vs INPUT POWER (0) or OUTPUT POWER (1) =  "
4390      Ques5$="MAXIMUN DELTA-GAIN = "
4400      Ques6$="MINIMUM DELTA-GAIN = "
4410      FOR J=1 TO 10
4420                FOR K=1 TO 20
4430                          Y(J,K)=De_gain(J,K)
4440                NEXT K
4450      NEXT J
4460      GOSUB Pt_delta
4470      IF Ans$="Y" THEN GOTO Pt_del_gain
4480      PAUSE
4490      GINIT
4500      GRAPHICS OFF
```

```
4510      GOTO Setkeys
4520 !
4530 Pt_delta:!
4540 !
4550      PRINT Label1$;
4560      INPUT Del_gain_fg
4570      PRINT Del_gain_fg
4580      IF Del_gain_fg=1 THEN GOTO Pto
4590      PRINT Ques2$;
4600      INPUT Xamax
4610      PRINT Xamax
4620      PRINT Ques1$;
4630      INPUT Xamin
4640      PRINT Xamin
4650      FOR J=1 TO 10
4660                FOR K=1 TO 20
4670                          X(J,K)=Pin(J,K)
4680                NEXT K
4690      NEXT J
4700      GOTO Plot_0
4710 Pto:!
4720      PRINT Ques3$;
4730      INPUT Xamax
4740      PRINT Xamax
4750      PRINT Ques4$;
4760      INPUT Xamin
4770      PRINT Xamin
4780      FOR J=1 TO 10
4790                FOR K=1 TO 20
4800                          X(J,K)=Pout(J,K)
4810                NEXT K
4820      NEXT J
4830 Plot_0:!
4840      Xa_range=Xamax-Xamin
4850      Xatick=(Xamax-Xamin)/Xa_range
4860 Plot_1: !
4870      PRINT Ques5$;
4880      INPUT Yamax
4890      PRINT Yamax
4900      PRINT Ques6$;
4910      INPUT Yamin
4920      PRINT Yamin
4930      GINIT
4940      GRAPHICS OFF
4950      GRAPHICS ON
4960      Ya_range=Yamax-Yamin
4970      Yatick=(Yamax-Yamin)/Ya_range
4980      CSIZE 4
4990      LORG 6
5000      Name_date$="T.C.CHENG  APRIL 2,1984"
```

```
5010      INPUT "NAME & DATE = ",Name_data$
5020      Ans$="N"
5030      INPUT "PLOTTER IS EXTERNAL ? ( Y/N ) <N> ",Ans$
5040      IF Ans$="Y" THEN GOTO Ext
5050      PLOTTER IS 3,"INTERNAL"
5060      FOR I=-.25 TO .25 STEP .1
5070                MOVE X_gdu_max/2+I,Y_gdu_max
5080                IF Del_gain_fg=0 THEN
5090                          LABEL Text2$
5100                ELSE
5110                          LABEL Text1$
5120                END IF
5130      NEXT I
5140      GOTO Cont11
5150 Ext:PLOTTER IS 705,"HPGL"
5160      MOVE X_gdu_max/2+I,Y_gdu_max
5170      IF Del_gain_fg=0 THEN
5180                LABEL Text2$
5190      ELSE
5200                LABEL Text1$
5210      END IF
5220 Cont11:CSIZE 3
5230      PENUP
5240      BEEP
5250      PRINT "CHANGE COLOUR ? THEN PRESS 'CONT'"
5260      PAUSE
5270      MOVE X_gdu_max/2,Y_gdu_max*.94
5280      LABEL "      ";Name_date$
5290      PENUP
5300      BEEP
5310      PRINT "CHANGE COLOUR ? THEN PRESS 'CONT'"
5320      PAUSE
5330      DEG
5340      LDIR 90
5350      CSIZE 3.5
5360      MOVE 3.0,Y_gdu_max/2
5370      LABEL Labely$
5380      LORG 4
5390      LDIR 0
5400      MOVE X_gdu_max/2,.07*Y_gdu_max
5410      IF Del_gain_fg=0 THEN
5420                LABEL Label2$
5430      ELSE
5440                LABEL Label1$
5450      END IF
5460      VIEWPORT .1*X_gdu_max,.98*X_gdu_max,.15*Y_gdu_max,.9*Y_gdu_max
5470      WINDOW Xamin,Xamax,Yamin,Yamax
5480      CSIZE 3
5490      CLIP ON
5500      AXES Xatick,Yatick,Xamin,Yamin,Xa_range,Ya_range,3
```

```
5510      AXES -Xatick,-Yatick,Xamax,Yamax,Xa_range,Ya_range,3
5520      LORG 6
5530      CLIP OFF
5540      FOR I=Xamin TO Xamax
5550                MOVE I,Yamin
5560                LABEL USING "#,K";I
5570      NEXT I
5580      LORG 8
5590      FOR I=Yamin TO Yamax
5600                MOVE Xamin-.2*Xatick,I
5610                LABEL USING "#,K";I
5620      NEXT I
5630      LORG 5
5640      CSIZE 2
5650      CLIP ON
5660      FOR M=1 TO Freq_number
5670                MOVE X(M,1),Y(M,1)
5680                FOR I=1 TO Cw_step_number
5690                          PLOT X(M,I),Y(M,I)
5700                NEXT I
5710                FOR I=Cw_step_number-5 TO Cw_step_number
5720                MOVE X(M,I),Y(M,I)
5730                LABEL M
5740                NEXT I
5750      NEXT M
5760      Label_ay=3*Yatick+Yamin
5770      CSIZE 3
5780      MOVE Xamin+5.2*Xatick,Label_ay
5790      LABEL "         FREQ(GHz)  GAIN(dB)    "
5800      FOR J=1 TO Freq_number
5810                MOVE Xamin+5*Xatick,Label_ay-J*.5*Yatick
5820                LABEL USING Image5;Freq(J);G(J)
5830      NEXT J
5840      CLIP OFF
5850      PENUP
5860      PRINT "CHANGE SCALE ? Y/N ? ";
5870      Ans$="N"
5880      INPUT Ans$
5890      PRINT Ans$
5900      IF Ans$="Y" THEN GOTO Plot_1
5910      PRINT " PLOT AGAIN ? ";
5920      Ans$="N"
5930      INPUT Ans$
5940      PRINT Ans$
5950      RETURN
5960 '
5970 Pt_del_phase:'
5980 '
5990      Label$=" DELTA-PHASE ( DEGREES )"
6000      Text1$=" DELTA-PHASE v.s. OUTPUT POWER "
```

```
6010      Text2$=" DELTA-PHASE v.s. INPUT POWER "
6020      Label$="DELTA-PHASE vs INPUT POWER (0) or OUTPUT POWER (1) = "
6030      Ques5$="MAXIMUN DELTA-PHASE = "
6040      Ques6$="MINIMUM DELTA-PHASE = "
6050      FOR J=1 TO 10
6060                FOR K=1 TO 20
6070                          Y(J,K)=De_phase(J,K)
6080                NEXT K
6090      NEXT J
6100      GOSUB Pt_delta
6110      IF Ans$="Y" THEN GOTO Pt_del_phase
6120      PAUSE
6130      GINIT
6140      GRAPHICS OFF
6150      GOTO Setkeys
6160 Pt_pin_pout:!
6170      PRINT "INPUT DATA FROM EXTERNAL Y/N (N) ";
6180      Ans$="N"
6190      INPUT Ans$
6200      PRINT Ans$
6210      IF Ans$="Y" THEN GOTO Ex_pipo
6220      Text1$=" OUTPUT POWER v.s. INPUT POWER "
6230      PRINT Ques2$;
6240      INPUT Xamax
6250      PRINT Xamax
6260      PRINT Ques1$;
6270      INPUT Xamin
6280      PRINT Xamin
6290      Xa_range=Xamax-Xamin
6300      Xatick=(Xamax-Xamin)/Xa_range
6310      PRINT Ques3$;
6320      INPUT Yamax
6330      PRINT Yamax
6340      PRINT Ques4$;
6350      INPUT Yamin
6360      PRINT Yamin
6370      Ya_range=Yamax-Yamin
6380      Yatick=(Yamax-Yamin)/Ya_range
6390      CSIZE 4
6400      LORG 6
6410      PRINT "NAME & DATE = ";
6420      Name_date$="T.C.CHENG  APRIL 2,1984"
6430      INPUT Name_date$
6440      PRINT Name_date$
6450      PRINT "PLOTTER IS EXTERNAL ? ( Y/N ) <N> "
6460      INPUT Ans$
6470      IF Ans$="Y" THEN GOTO Ext2
6480      PLOTTER IS 3,"INTERNAL"
6490      FOR I=-.25 TO .25 STEP .1
6500                MOVE X_gdu_max/2+I,Y_gdu_max
```

```
6510                LABEL Text1$
6520     NEXT I
6530     GOTO Cont1
6540 Ext2:PLOTTER IS 705,"HPGL"
6550     MOVE X_gdu_max/2+I,Y_gdu_max
6560     LABEL Text1$
6570 Cont1:CSIZE 3
6580     PENUP
6590     BEEP
6600     PRINT "CHANGE COLOUR ? THEN PRESS 'CONT'"
6610     PAUSE
6620     MOVE X_gdu_max/2,Y_gdu_max*.94
6630     LABEL "        ";Name_date$
6640     PENUP
6650     BEEP
6660     PRINT "CHANGE COLOUR ? THEN PRESS 'CONT'"
6670     PAUSE
6680     DEG
6690     LDIR 90
6700     CSIZE 3.5
6710     MOVE 3.0,Y_gdu_max/2
6720     LABEL Label$1$
6730     LORG 4
6740     LDIR 0
6750     MOVE X_gdu_max/2,.07*Y_gdu_max
6760     LABEL Label$2$
6770     VIEWPORT .1*X_gdu_max,.98*X_gdu_max,.15*Y_gdu_max,.9*Y_gdu_max
6780     WINDOW Xamin,Xamax,Yamin,Yamax
6790     CSIZE 3
6800     CLIP ON
6810     AXES Xatick,Yatick,Xamin,Yamin,Xa_range,Ya_range,3
6820     AXES -Xatick,-Yatick,Xamax,Yamax,Xa_range,Ya_range,3
6830     LORG 6
6840     CLIP OFF
6850     FOR I=Xamin TO Xamax
6860               MOVE I,Yamin
6870               LABEL USING "#,K";I
6880     NEXT I
6890     LORG 8
6900     FOR I=Yamin TO Yamax
6910               MOVE Xamin-.2*Xatick,I
6920               LABEL USING "#,K";I
6930     NEXT I
6940     LORG 5
6950     CSIZE 2
6960     FOR M=1 TO Freq_number
6970               MOVE Pin(M,1),Pout(M,1)
6980               FOR I=1 TO Cw_step_number
6990                         PLOT Pin(M,I),Pout(M,I)
7000               NEXT I
```

```
7010                FOR I=Cw_step_number-5 TO Cw_step_number
7020                MOVE Pin(M,I),Pout(M,I)
7030                LABEL M
7040                NEXT I
7050      NEXT M
7060      CSIZE 3
7070      MOVE Xamin+5*Xatick,4*Yatick
7080      LABEL "         FREQ(GHz)  GAIN(dB)    "
7090      FOR J=1 TO Freq_number
7100                MOVE Xamin+5*Xatick,Yamin+(5-J)*Yatick
7110                LABEL USING Image6;J;Freq(J);G(J)
7120      NEXT J
7130      PENUP
7140      PAUSE
7150      GOTO Setkeys
7160 Ex_pipo:!
7170      READ Freq_number,Cw_step_number
7180      PRINT Freq_number;Cw_step_number
7190      FOR M=1 TO Freq_number
7200                READ Freq(M),G(M)
7210                PRINT Freq(M);G(M)
7220                FOR J=1 TO Cw_step_number
7230                          READ Pin(M,J),Pout(M,J),De_gain(M,J),De_phase(M,J)
7240                          PRINT Pin(M,J);Pout(M,J);De_gain(M,J);De_phase(M,J)
7250                NEXT J
7260      NEXT M
7270      END
```

CHAPTER 3 INTER-ACTIVE COMPUTER STUDY of INSTABILITY in GaAs DEVICES

3.1 S-PARAMETERS

The use of S-parameters for characterization of small-signal, linear microwave devices and circuits is well known(1). S-parameters are a valuable tool in analytic design of linear microwave circuits(2), because of ease of measurement and the convenience of their use. Analytic design procedure, using S-parameters, are well developed for small-signal transistor amplifiers. A block diagram of single stage GaAs FET amplifier is shown in Figure 3.1.1.

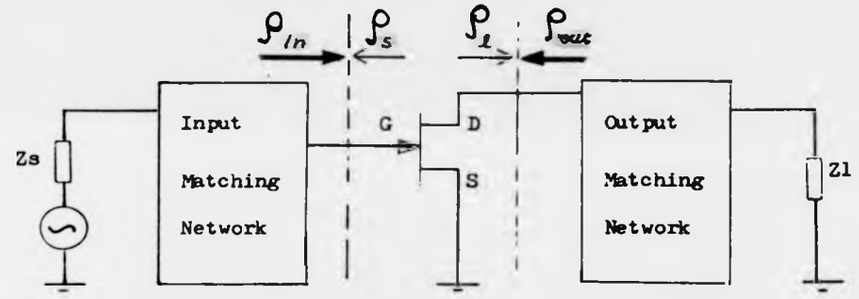


Figure 3.1.1 A block diagram of a single stage GaAs FET amplifier

Input reflection coefficient ρ_{in} and output reflection coefficient ρ_{out} of a transistor with matching circuits are represented using the S-parameters of the transistor as follows.

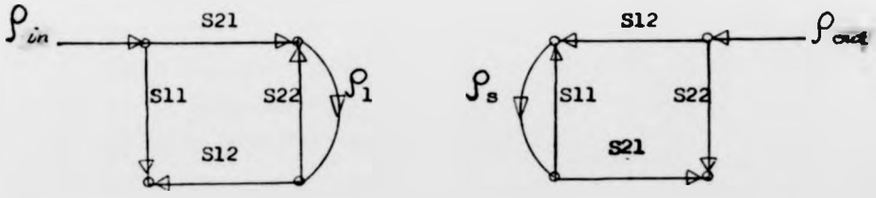


Figure 3.1.2. Flow graph for calculating ρ_{in} and ρ_{out}.

Where: S11- Input reflection coefficient when terminated at outputport.
S22- Output reflection coefficient when terminated at inputport.
S12- Reverse transmission coefficient when terminated at inputport.
S21- Forward transmission coefficient when terminated at outputport.
ρ_s- Reflection coefficient of the source.
ρ_l- Reflection coefficient of the load.
Zs- Source impedance.
Zl- Load impedance.

Flow graph techniques can be used to determine the overall response of a network once the component parts are known. A flow graph reduction technique known as " Mason's non-touching-loop rule " (3) say that the overall response of a network is the sum of paths which energy can flow through the network. Therefore, from signal flow graph as shown in Figure 3.1.2 yields

$$\rho_{in} = S11 + \frac{S21 \cdot S12 \cdot \rho_l}{1 - S22 \cdot \rho_l} \qquad (3.1.1)$$

$$\rho_{out} = S22 + \frac{S12 \cdot S21 \cdot \rho_s}{1 - S11 \cdot \rho_s} \qquad (3.1.2)$$

3.2 STABILITY OF A TWO PORTS NETWORK

One important parameter in the design of microwave amplifiers is that of stability. A ρ_s or ρ_l which cause the magnitude of ρ_{out} or ρ_{in} to be larger than unity makes the network unstable, on the other hand, a ρ_l or ρ_s which cause the magnitude of ρ_{in} and ρ_{out} to be equal to or smaller than unity makes the circuit stable.

The transducer gain, Gt, of a transistor is defined as(4):

$$Gt = \frac{|S21|^2 (1-|\rho_s|^2)(1-|\rho_l|^2)}{|(1-S11\rho_s)(1-S22\rho_l) - s12\ S21\rho_s\rho_l|^2} \quad (3.2.1)$$

When ρ_s and ρ_l are image matched to the transistor's two ports, the gain can be maximized to give:

$$G_{max} = \frac{|S21|^2}{(1-|S11|^2)(1-|S22|^2)} \quad (3.2.2)$$

Where $\rho_s = S11^*$ and $\rho_l = S22^*$, $S11^*$ and $S22^*$ being the complex conjugate reflection coefficients of S11 and S22 respectively.

In Eqn. (3.2.2), S12 is assumed to be zero, i.e. the device is assumed unilateral.

The S-parameters also determine Rollett's stability factor, K(5):

$$K = \frac{1 - |S11\ S22 - S12\ S21|^2 - |S11|^2 - |S22|^2}{2|S12\ S21|} \quad (3.2.3)$$

If K is larger than unity, an optimum combination of ρ_s and ρ_l can simultaneously match the transistor's two ports to maximize the gain(6).

If K is smaller than unity, the transistor is only conditionally stable, some combinations of source and load impedances will cause the transistor to oscillate. Therefore ρ_s and ρ_l must be carefully chosen to operate the device in a stable region (6,7). For these transistors, the maximum avilable gain is not defined, as in principle any desired gain can be achieved by operating arbitrarily close to oscillation.

PLOTTING STABILITY CIRCLES

Stability circles can be plotted directly on a Smith chart. These separate the output or input planes into stable and unstable regions. A stability circle plotted on the output plane indicates the values of all loads that provide negative real input impedance, thereby causing the circuit to oscillate. A similar circle can be plotted on the input plane which indicates the values of all loads that provide negative real output impedance and again cause oscillation. A negative real impedance is defined as a reflection coefficient which has a magnitude that is greater than unity.

The regions of instability occur within the circles whose centers and radii are expressed by (2)

$$r_{s1} = \frac{C_1^*}{|S11|^2 - |\Delta|^2} \qquad (3.2.4)$$

$$R_{s1} = \frac{|S12 \cdot S21|}{|S11|^2 - |\Delta|^2} \qquad (3.2.5)$$

$$r_{s2} = \frac{C_2^*}{|S22|^2 - |\Delta|^2} \qquad (3.2.6)$$

$$R_{s2} = \frac{|S12 \cdot S21|}{|S22|^2 - |\Delta|^2} \qquad (3.2.7)$$

Where r_{s1} - center on the input plane
R_{s1} - radius on the input plane
r_{s2} - center on the output plane
R_{s2} - radius on the output plane

$$C_1 = S11 - \Delta \cdot S22^* \qquad (3.2.8)$$

$$C_2 = S22 - \Delta \cdot S11^* \qquad (3.2.9)$$

$$\Delta = S11 \cdot S22 - S12 \cdot S21 \qquad (3.2.10)$$

In these equations the asterisk represents the complex conjugate value.

PLOTTING CONSTANT GAIN CIRCLES

The design of an amplifier where K is positive and greater than unity is relatively simple since these conditions indicate that the device is unconditionally stable under any load conditions. All one needs to do is to compute the values of R_{ms} and R_{ml} that will simultaneously match both the input and output ports and give the maximum power gain of the device (2).

$$R_{ms} = C_1^* \left[\frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2|C_1|^2} \right] \qquad (3.2.11)$$

$$R_{ml} = C_2^* \left[\frac{B_2 \pm \sqrt{B_2 - 4|C_2|^2}}{2|C_2|^2} \right] \qquad (3.2.12)$$

Where R_{ms} - reflection coefficient of the source impedence required to conjugately match the input of the transistor.

R_{ml} - reflection coefficient of that load impedance required to conjugately match the output of the transistor.

$$B_1 = 1 + |S11|^2 - |S22|^2 - |\Delta|^2 \qquad (3.2.13)$$

$$B_2 = 1 + |S22|^2 - |S11|^2 - |\Delta|^2 \qquad (3.2.14)$$

If the compute value on B_1 is negative, then the plus sign should be used in front of the radical in equation (3.2.11). Conversely, if B_1 is positive, then the negative sign should be used. This also applies in equation (3.2.12). By using the appropriate sign only one answer will be possible in either equation and a value of less than unity will be computed.

The design method when K is less than unity is to first select the the desired gain and calculate the locus of all load impedances that will yield the desired gain when the transistor input is conjugate matched. This locus is the constant gain circle on a Smith chart.

The center and the radius of the constant gain circle are given by the following equations (2)

$$r_{02} = \left[\frac{G}{1 + D_2 G}\right] C_2^* \qquad (3.2.15)$$

$$R_{02} = \frac{\left(1 - 2K|S12S21|G + |S12S21|^2 G^2\right)^{1/2}}{1 + D_2 G} \qquad (3.2.16)$$

where

r_{02} - the center of the constant gain circle on the output plane.
R_{02} - the radius of the constant gain circle on the output plane.

$$D_2 = |S22|^2 - |\Delta|^2 \qquad (3.2.17)$$

$$G = \frac{Gp}{|S21|^2} \qquad (3.2.18)$$

Gp - the desired total amplifier gain (numeric)

If the compute value on B_1 is negative, then the plus sign should be used in front of the radical in equation (3.2.11). Conversely, if B_1 is positive, then the negative sign should be used. This also applies in equation (3.2.12). By using the appropriate sign only one answer will be possible in either equation and a value of less than unity will be computed.

The design method when K is less than unity is to first select the the desired gain and calculate the locus of all load impedances that will yield the desired gain when the transistor input is conjugate matched. This locus is the constant gain circle on a Smith chart.

The center and the radius of the constant gain circle are given by the following equations (2)

$$r_{02} = \left[\frac{G}{1 + D_2 G}\right] C_2^* \qquad (3.2.15)$$

$$R_{02} = \frac{(1 - 2K|S12S21|G + |S12S21|^2 G^2)^{1/2}}{1 + D_2 G} \qquad (3.2.16)$$

where

r_{02} - the center of the constant gain circle on the output plane.
R_{02} - the radius of the constant gain circle on the output plane.

$$D_2 = |S22|^2 - |\Delta|^2 \qquad (3.2.17)$$

$$G = \frac{Gp}{|S21|^2} \qquad (3.2.18)$$

Gp - the desired total amplifier gain (numeric)

After a load that falls on the desired constant gain circle has been selected, a source impedance is selected to achieve the desired gain. The value for the generator (or source) impedance that simultaneously matches the input load is given by (2)

$$r_1 = \left[\frac{S11 - r_2}{1 - r_2 \cdot S22} \right]^* \qquad (3.2.19)$$

where r_2 is the reflection coefficient of the load picked.

The stability circles separate the stable regions on the Smith chart from the potentially unstable regions. Whether the inside or the outside of the load stability circle is the region of stability, it can be determined by calculating the input reflectionn coefficient ρ_{in} corrsponding to any load impedance Z_1 inside the circle using equation (3.1.1). If $|\rho_{in}|$ is greater than unity, the inside of the circle is potentially unstable.

A similar technique can be applied to the output reflection coefficient ρ_{out} , using equation (3.1.2).

For the case where K<1 the maximum stable gain or MSG of the transistor can be calculated as

$$MSG = \frac{|S21|}{|S12|} \qquad (3.2.20)$$

In general, where $K \geq 1$, the maximum available gain (MAG)

$$MAG = \frac{|S21|}{|S12|} \left(K - \sqrt{K-1} \right) \qquad (3.2.21)$$

Thus MAG = MSG when K = 1 and the MSG is the gain that can be obtained from the transistor when the input and output reflection coefficients fall on the boundaries of the instability regions.

For a two-port with the stability factor K greater than unity, it is possible to simultaneously conjugate match the two-port to produce the maximum available gain. The condition for simultaneous conjugate match can be inspected from equations(3.1.1) and (3.1.2), yield:

$$\rho_{in} = S11 + \frac{S21\ S12\ \rho_l}{1 - S22\ \rho_l} = \rho_s^* \qquad (3.2.22)$$

$$\rho_{out} = S22 + \frac{S12\ S21\ \rho_s}{1 - S11\ \rho_s} = \rho_l^* \qquad (3.2.23)$$

The load impedances R_{ms} and R_{ml} under the simultaneous conjugate matched condition are given by equations (3.2.11) and (3.2.12).

The transistor can then be modeled either in series form or in parallel form as shown in Figure 3.2.

Series form Parallel form

Figure 3.2 Series and parallel equivalents of an impedance

The conversion formulae for series and parallel equivalents are as follow:

$$R_p = R_s \times \left[1 + \left(\frac{X_s}{R_s}\right)^2\right]; \qquad X_p = \frac{R_s \times R_p}{X_s} \qquad (3.2.24)$$

$$R_s = R_p \div \left[1 + \left(\frac{R_p}{X_p}\right)^2\right]; \qquad X_s = \frac{R_s \times R_p}{X_p} \qquad (3.2.25)$$

3.3 Computer program

An inter-active computer program has been developed by the author, since the stability of the transistor is of vital importance for the design of an amplifier. The program is written in Basic language for the HP9845 desktop computer.

The program structure consists of three control levels. See Figure 3.3.1.

Control level 1: There are three control keys available in this level. By pressing Key " 0 " on the keyboard of the computer, a new data set of S-parameters can be created and stored into tne data tape. Key " 24 " controls . plotting any value of normalized resistance or reactance on the Smith chart, it is convenient to locate any normalized impedance on the chart. Tne third control keys is Key " 1 " , the computer will firstly reload tne specified S-parameters data into the memory from the storage tape. The S-parameters can be either listed on the monitor screen or printed as a hard copy. Overlaying previous calculating curves are also provided, before it goes to Sub-control level 2. The flow chart of control no. 1 is shown in Figure 3.3.2.

Control level 2: The flow chart of control level no. 2 is found in Figure 3.3.3. A typical control table for FSX51WF is as follows:

CONTROL	Action
0	Goto Main Control
1	2000 MHz
2	3000 MHz
3	4000 MHz
4	5000 MHz
5	6000 MHz
6	7000 MHz
7	8000 MHz
8	9000 MHz
09	10000 MHz
10	11000 MHz
11	12000 MHz
12	Interpolation of S-parameters
13	Plot S-parameters on the Smith chart
14	Plot Smith chart as a background
15	Plot S12 & S21 scaling background.

By typing numeric number " 0 ", it exits to Control level no.1.
By typing any numeric number from " 1 " to " N " (which is " 11 " in this example for FSX51WF), it goes to Control level no.3.
Interpolation of S-parameters is made by numeric number " N+1 ",
The following numeric control numbers give facilities for plotting S-parameters on the Smith chart background for S11 and S22 as in Figure 3.3.5 , for S12 and S21 is shown in Figure 3.3.6 with polar scaling background.

Control level no.3: The Flow chart for tnis control level is shown Figure 3.3.4. In this control level, a computation start with calculating of stability K factor at desired single frequency. Stability circles information are given either at the input or output ports. An example of the instabilities regions (shaded areas) is shown in Figure 3.3.7, for FSX51WF at the input port. Constant gain circles can be plotted with several desired gain values, Figure 3.3.8 is an example for FSX51WF with its constant gain circles at 6GHz, 8GHz and 10GHz. For K greater unity, based on simultaneously matched both at the input and output ports, the device can be modeled in either series form or parallel form, Figure 3.3.9 is an example for NE72089 with its model at 8GHz.

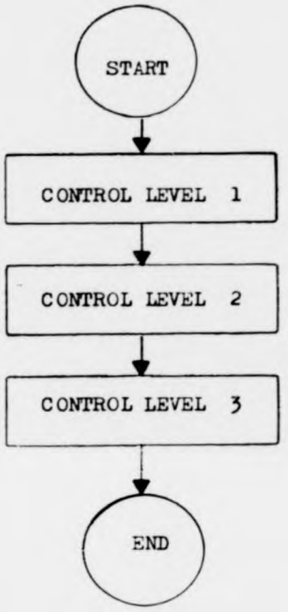


Figure 3.3.1 Program structure

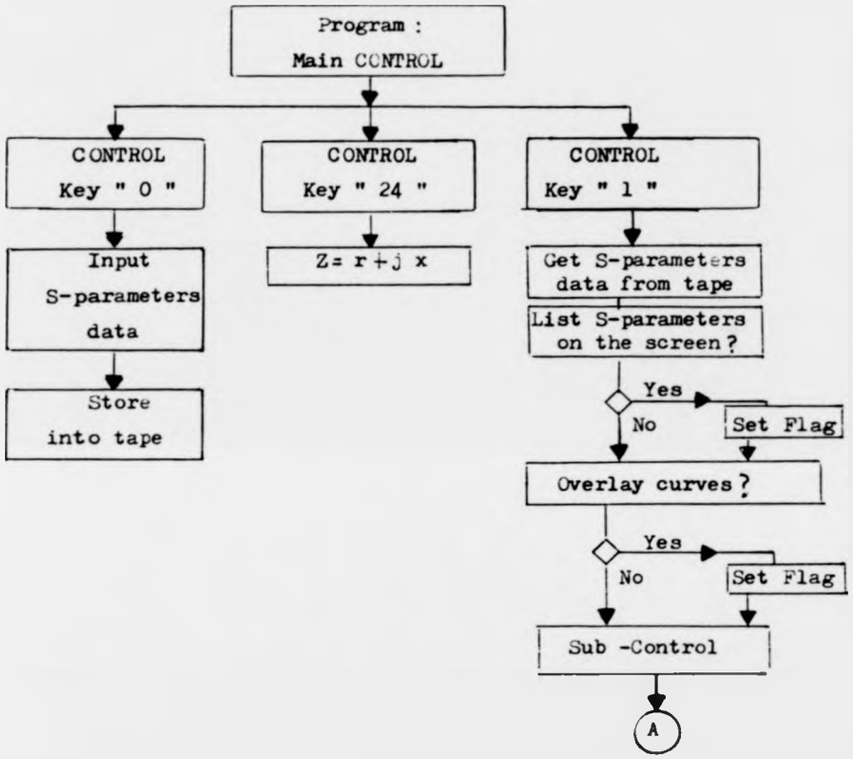


Figure 3.3.2 Flow chart for Control Level no.1

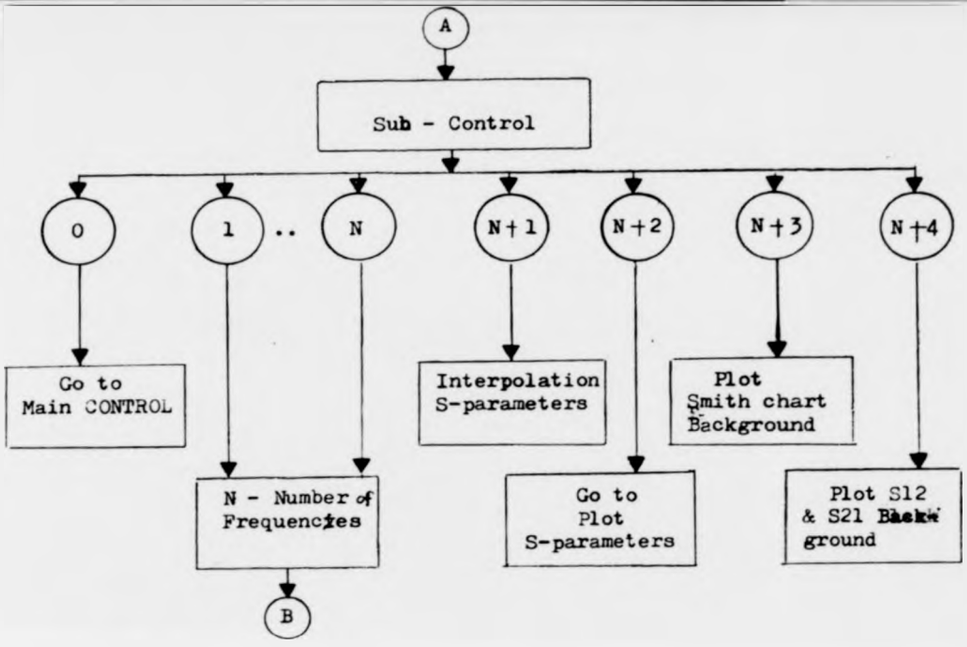
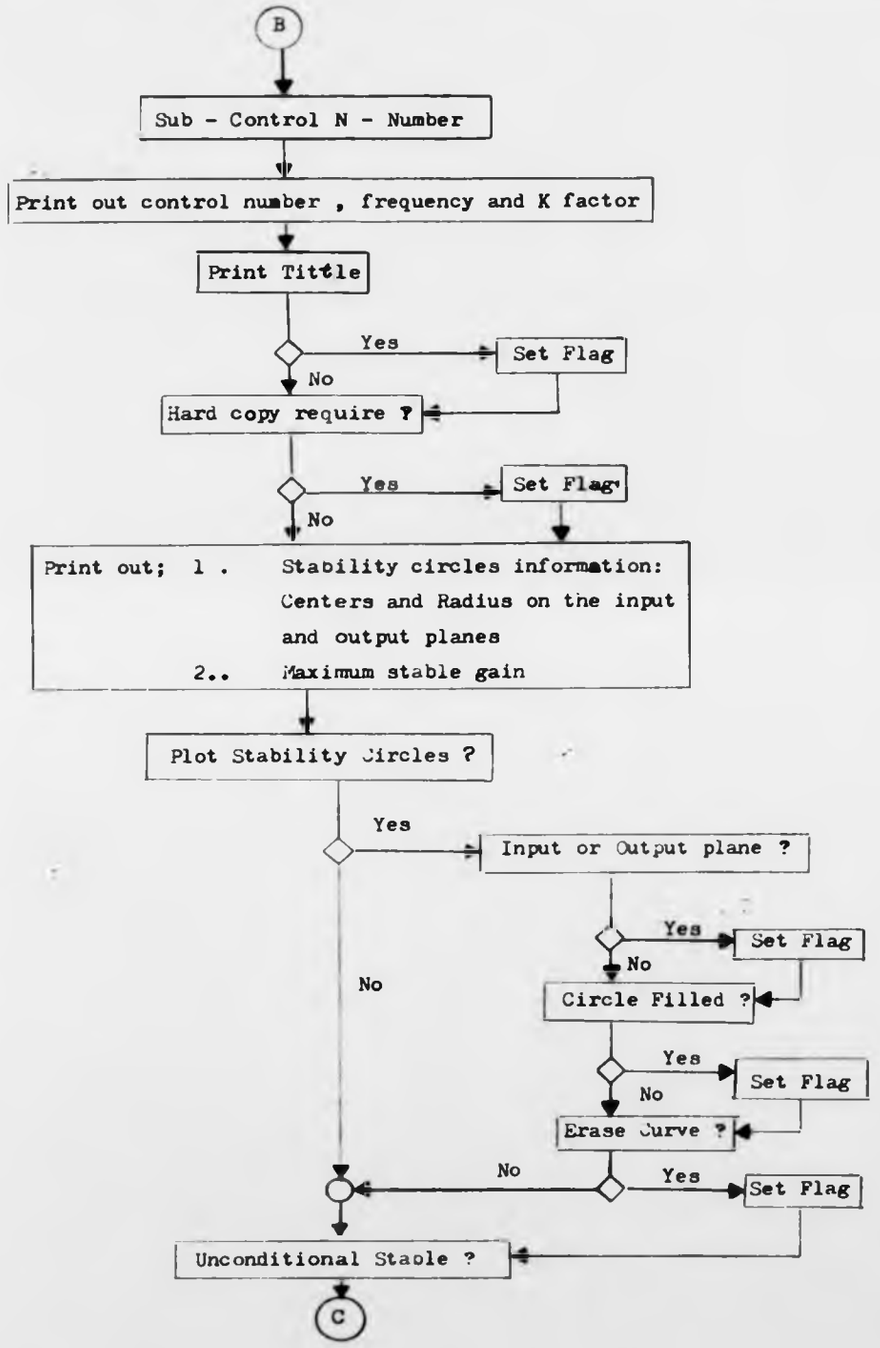


Figure 3.3.3 Flow chart for Control Level no. 2


B
Sub - Control N - Number
Print out control number , frequency and K factor
Print Tittle
Yes
Set Flag
No
Hard copy require ?
Yes
Set Flag
No
Print out; 1 . Stability circles information:
Centers and Radius on the input
and output planes
2.. Maximum stable gain
Plot Stability Circles ?
Yes
Input or Output plane ?
Yes
Set Flag
No
Circle Filled ?
Yes
Set Flag
No
Erase Curve ?
No
Yes
Set Flag
No
Unconditional Staole ?
C

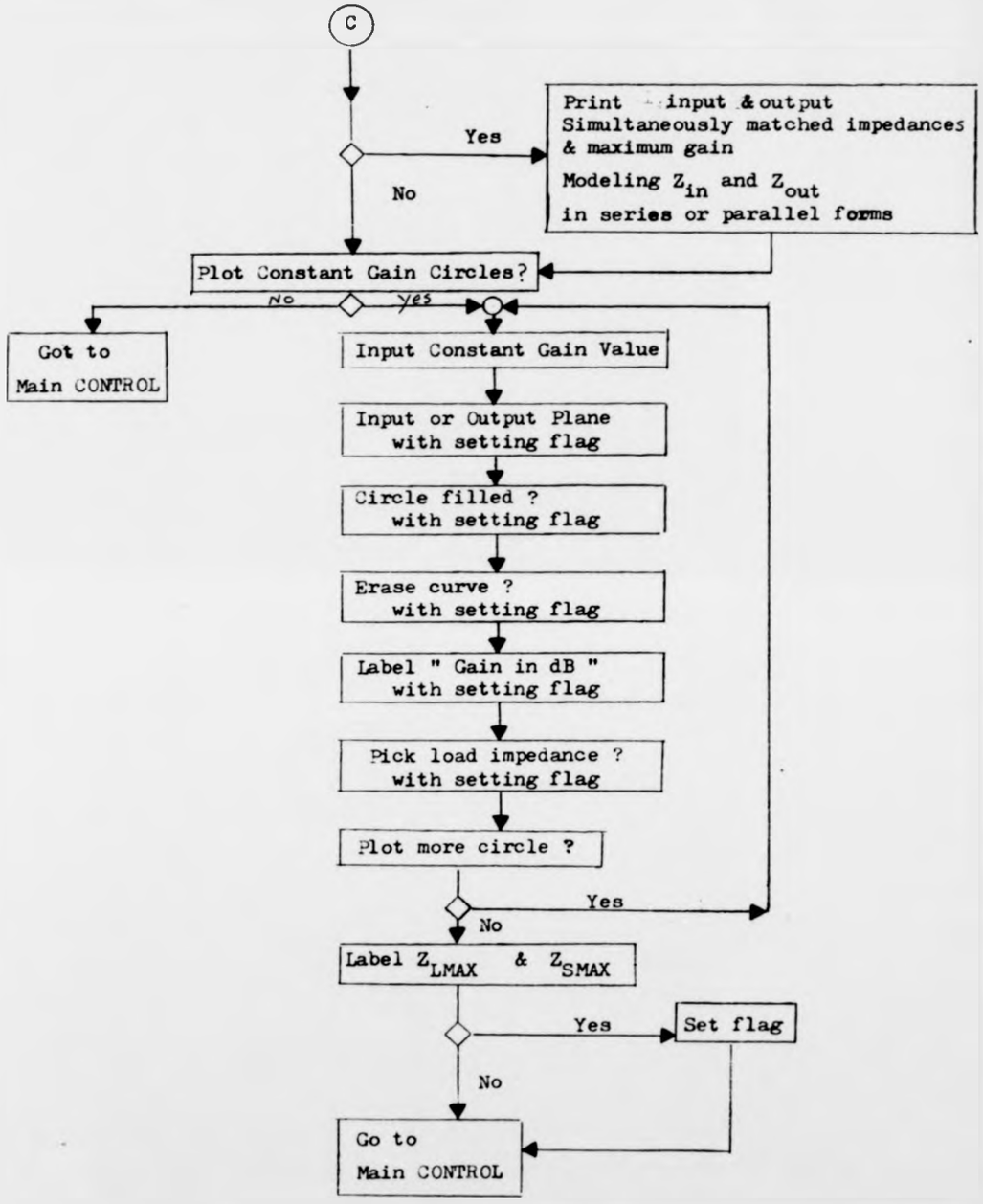


Figure 3.3.4 Flow chart for Control Level no.3

FSX51X (Vds= 8.00 V Ids= 30.00 ma) : S-parameters

FREQ(Mhz)	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
2000.00	.933	-52.00	2.658	130.00	.029	53.00	.779	-32.00
3000.00	.899	-71.00	2.357	110.00	.035	39.00	.784	-42.00
4000.00	.859	-83.00	2.205	99.00	.038	33.00	.801	-52.00
5000.00	.815	-93.00	2.102	85.00	.041	26.00	.792	-57.00
6000.00	.772	-108.00	2.078	72.00	.049	15.00	.789	-63.00
7000.00	.646	-134.00	2.055	54.00	.056	-1.00	.742	-72.00
8000.00	.586	-163.00	2.060	30.00	.059	-26.00	.730	-88.00
9000.00	.559	174.00	2.031	6.00	.066	-46.00	.701	-112.00
10000.00	.532	155.00	1.765	-19.00	.071	-64.00	.711	-137.00
11000.00	.510	142.00	1.659	-39.00	.082	-78.00	.732	-153.00
12000.00	.456	113.00	1.605	-62.00	.103	-97.00	.707	-175.00

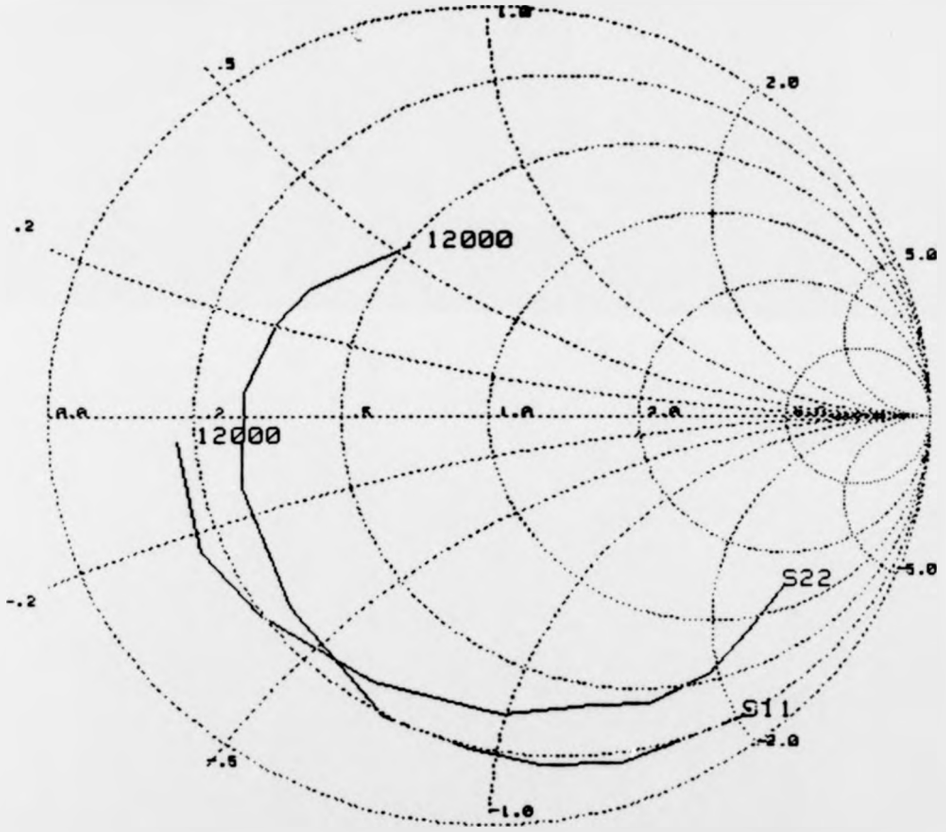


Figure 3.3.5 Plotting S11 and S22 on the Smith chart for FSX51WP

FSX51X (Vds= 8.00 V Ids= 30.00 ma) : S-parameters

FREQ(Mhz)	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
2000.00	.933	-52.00	2.658	130.00	.029	53.00	.779	-32.00
3000.00	.899	-71.00	2.357	110.00	.035	39.00	.784	-42.00
4000.00	.859	-83.00	2.205	99.00	.038	33.00	.801	-52.00
5000.00	.815	-93.00	2.102	85.00	.041	26.00	.792	-57.00
6000.00	.772	-108.00	2.078	72.00	.049	15.00	.789	-63.00
7000.00	.646	-134.00	2.055	54.00	.056	-1.00	.742	-72.00
8000.00	.586	-163.00	2.060	30.00	.059	-26.00	.730	-88.00
9000.00	.559	174.00	2.031	6.00	.066	-46.00	.701	-112.00
10000.00	.532	155.00	1.765	-19.00	.071	-64.00	.711	-137.00
11000.00	.510	142.00	1.659	-39.00	.082	-78.00	.732	-153.00
12000.00	.456	113.00	1.605	-62.00	.103	-97.00	.707	-175.00

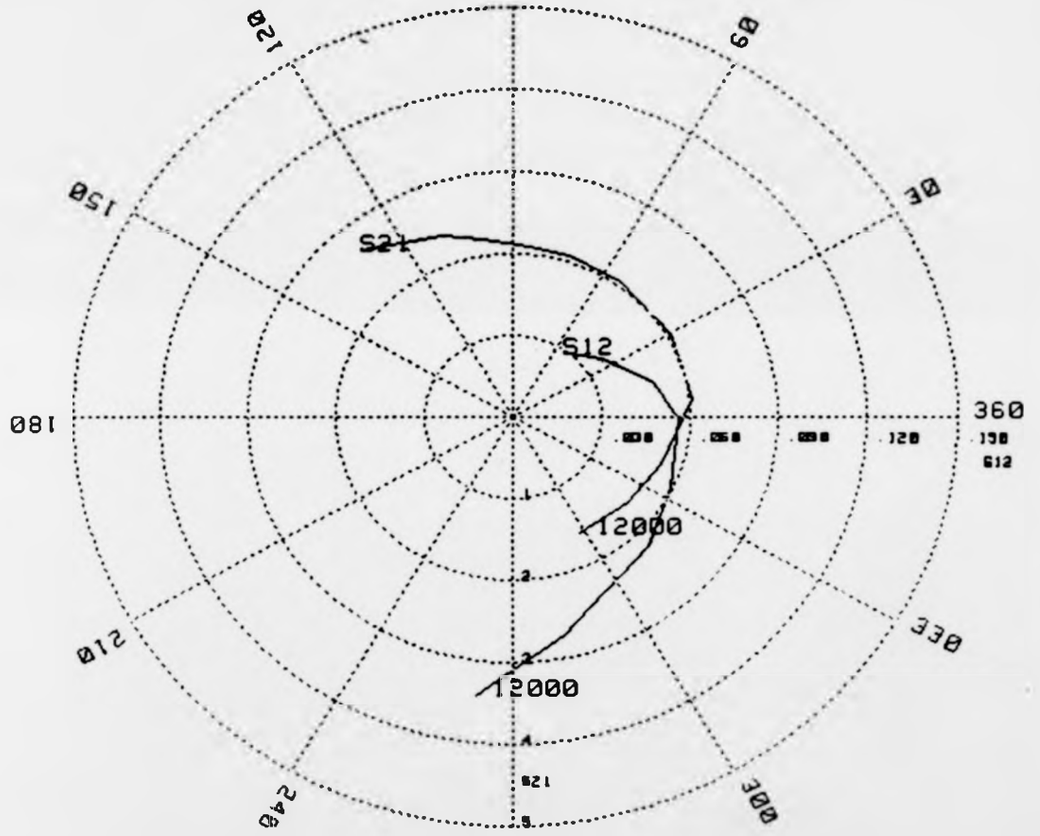


Figure 3.3.6 Plotting S12 and S21 on the Polar scaling background

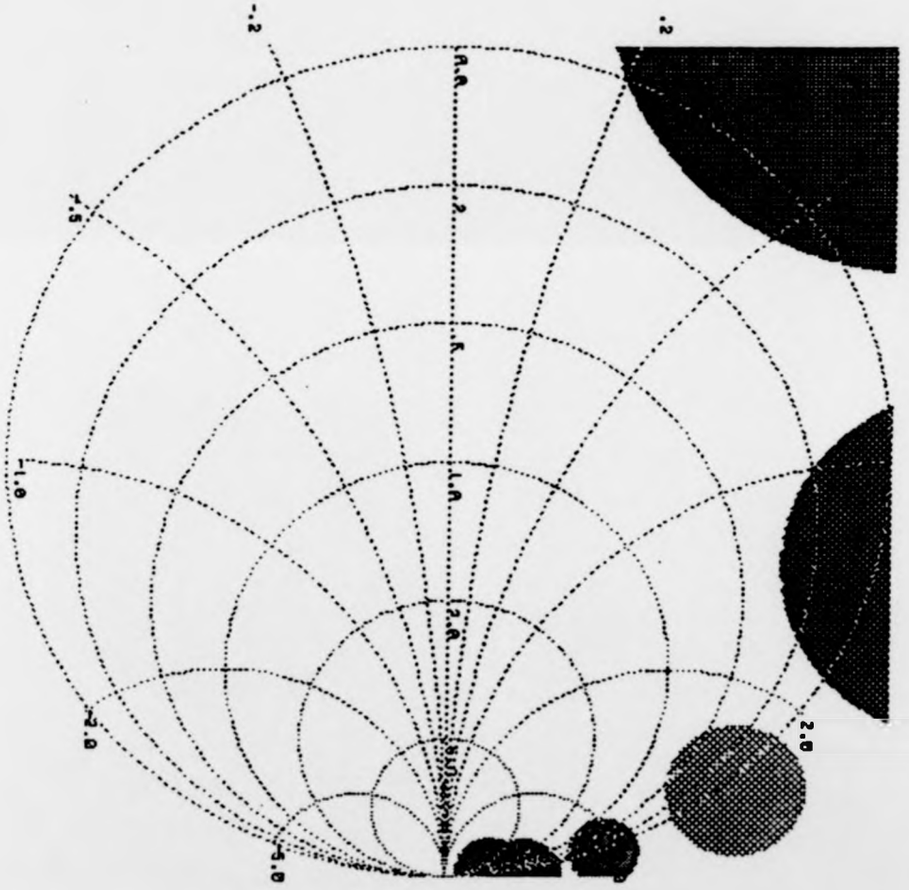


Figure 3.3.7 Typical unstable impedance regions for the FSX51WF
(From 2000 MHz to 7000 MHz)

FREQ(Mhz)	K	CSmag	CSang	Rads	CLmag	CLang	Radl
6000.00	1.12	1.78	177.91	.73	3.13	130.23	2.04

STABILITY region: UNCONDITION UNCONDITION

Rs1mod/Rs1: 1.777 / .726 ;Rs2mod/Rs2: 3.126 / 2.045 ; MSG = 13.692 dB

SIMULTANEOUS MATCH FOR MAXIMUM GAIN

FREQ(MHz)	Gmax (dB)	Input match Imp. ZSmag	ZSang	Output match Imp. ZLmag	ZLang
6000.00	11.56	.81	177.91	.72	130.23

STABILITY CIRCLE

	INPUT PLANE Origin		Radius	OUTPUT PLANE Origin		Radius
FREQ(Mhz)	K	CSmag	CSang	Rads	CLmag	CLang	Radl
10000.00	1.07	1.92	234.13	.89	2.04	181.49	1.01

STABILITY region: UNCONDITION UNCONDITION

Rs1mod/Rs1: 1.924 / .891 ;Rs2mod/Rs2: 2.043 / 1.007 ; MSG = 11.389 dB

SIMULTANEOUS MATCH FOR MAXIMUM GAIN

FREQ(MHz)	Gmax (dB)	Input match Imp. ZSmag	ZSang	Output match Imp. ZLmag	ZLang
10000.00	9.76	.84	234.13	.83	181.49

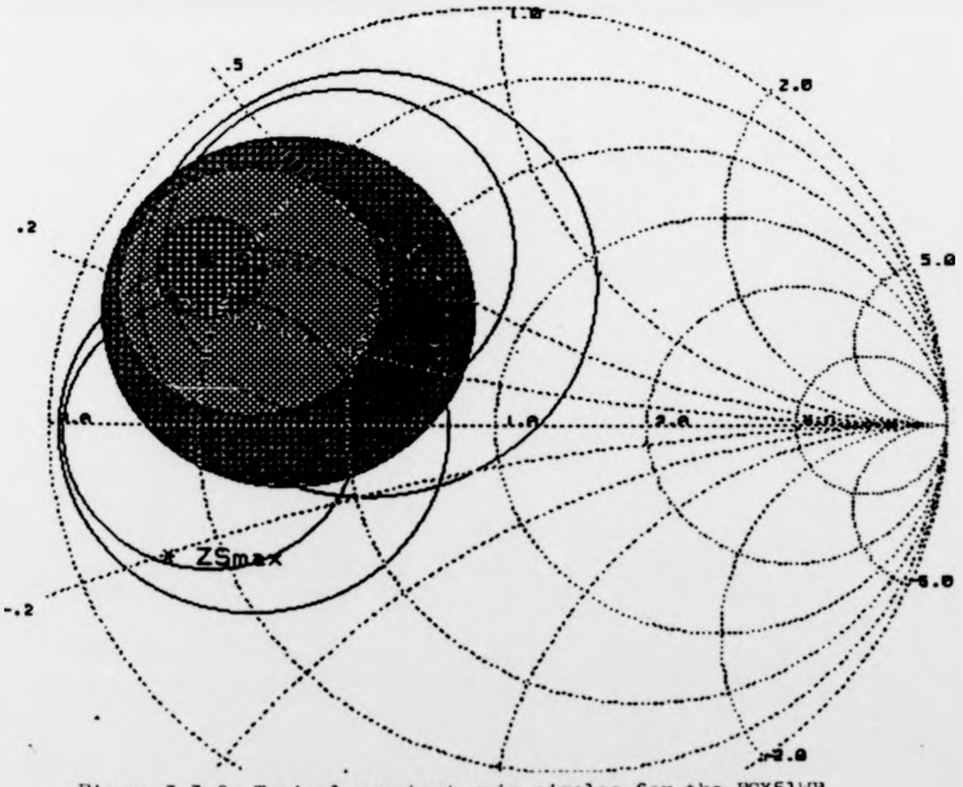


Figure 3.3.8 Typical constant gain circles for the FSX51WP at 6 GHz, 8GHz and 10 GHz

NE72089 (Vds= 4.00 V Ids= 30.00 ma)

		STABILITY CIRCLE					
		INPUT PLANE			OUTPUT PLANE		
		Origin		Radius	Origin		Radius
FREQ(Mhz)	K	CSmag	CSang	Rads	CLmag	CLang	Radl
8000.00	1.14	1.77	203.11	.71	2.09	149.61	1.02

STABILITY region: UNCONDITION UNCONDITION

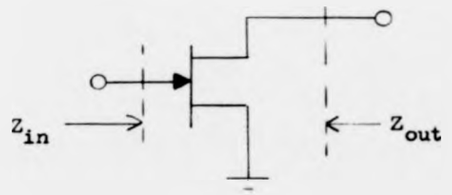
Rs1mod/Rs1: 1.770 / .714 ;Rs2mod/Rs2: 2.092 / 1.024 ; MSG = 12.486 dB

SIMULTANEOUS MATCH FOR MAXIMUM GAIN

FREQ(MHz)	Gmax (dB)	Input match Imp. ZSmag	ZSang	Output match Imp. ZLmag	ZLang
8000.00	10.23	.80	203.11	.77	149.61

INmatch-r= .112 INmatch-x=-.202 OUTmatch-r= .140 OUTmatch-x= .267
In 50 Ohms System : (Resistor in Ohms)
INmatch-R= 5.625 INmatch-CAP(pF)= 1.970 OUTmatch-R= 6.991 OUTmatch-IND(nH)= .265

Source-r= .112 Source-x= .202 Load-r= .140 Load-x=-.267
In 50 Ohms System : (Resistor in Ohms)
SE: Source-R= 5.625 Source-IND(nH)= .201
PA: Source-R= 23.756 Source-IND(nH)= .263
SE: Load-R= 6.991 Load-CAP(pF)= 1.492
PA: Load-R= 32.414 Load-CAP(pF)= 5.427



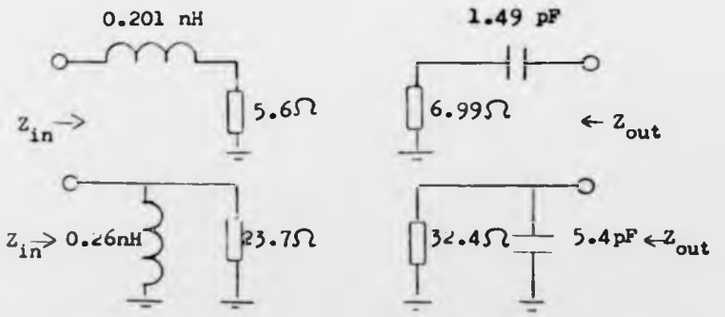


Figure 3.3.9 NE72089 input & output model at 8.0Ghz in series form and parallel form

3.4 REFERENCES

1. Hewlett-Packard Application Note 95, " S-parameters ... Circuit Analysis and Design, " September 1968.
2. Froehner, W.H." Quick Amplifier Design with Scattering Parameters," Electronics, October 16,1967.
3. Mason, S.J.,"Feedback Theory - Some Properties of Signal Flow Graphs, " Proc. IRE, Vol. 41, pp. 1144-1156, September 1953.
4. Hewlett-Packard Application Note 154, " S-parameter Design," April,1972,pp.11-13.
5. Rollett,J.," Stability and Power Gain Invariants of Linear Two Ports, " IRE Trans. on Circuit Theory, Vol. CT-9, pp.29-32, March 1967.
6. Bodway,G., " Two Port Power Flow Analysis Using Generalized Scattering Parameters, " Microwave Journal, Vol.10,pp.61-69, May 1967.
7. Gledhill,C. and Abulela,M.," Scattering Parameter Approach to the Design of Narrow- band Amplifier Employing Conditionally Stable Active Elements, " IEEE Trans. Microwave Theory and Techniques, Vol. MTT-22,pp.43-48,January 1974.

3.5 COMPUTER PROGRAM LISTING FOR INTER-ACTIVE COMPUTER STUDY OF INSTABILITY IN GaAs FET DEVICES

3.5 Program Listing

```
10   ! 30/04/1983 : Author:  T.C.CHENG
20   ! PROGRAM NAME : STBL
30   ! THIS PROGRAM IS USED TO CALCULATE STABILITY CIRCLES OF THE DEVICE
40   ! FOR MEASURED S_parameters
50   !
60     OPTION BASE 1
70     ALPHA
80     INTEGER K1,K2
90     SHORT S11m(20),S11a(20),S12m(20),S12a(20),Freq(20),X(20),Y(20)
100    SHORT S21m(20),S21a(20),S22m(20),S22a(20)
110    SHORT Cxxx(2),Cyyy(2),Rmodd(2)
120    SHORT Xrr(20,204),Yrr(20,204)
130    DIM Ans$[3],Data_file$[20],T1$[15]
140    DIM S1$[50],Ss$[50]
150 Image1:  IMAGE MDDDDD.DD,2X,MDD.DD,3X,MDDD.DD,3X,MDDD.DD,MDDD.DD,3X,MDDD.DD,
3X,MDDD.DD,MDDD.DD
160 Image2:  IMAGE MDDDDD.DD,2X,MDD.DD,3X,MDD.DD,2X,MDDD.DD,4X,MDD.DD,2X,MDDD.DD
170 Image3:  IMAGE MDDDD.DD,2X,MDD.DD,3X,MDD.DD,2X,MDDD.DD,4X,MDD.DD,2X,MDDD.DD
180 Image4:   IMAGE MDDDDD.DD,1X,MDD.DDD,1X,MDDD.DD,1X,MDD.DDD,1X,MDDD.DD,1X,MDD
.DDD,1X,MDDD.DD,1X,MDD.DDD,1X,MDDD.DD
190 Image5:   IMAGE MDDD,8X,MDDDDD.DD
191    PRINT " PLEASE WAIT program is loading... "
192    PRINT " "
200    DEG
210    FIXED 3
220    Data_file$="S2"
230 ! MASS STORAGE IS ":T14"
240    ASSIGN #1 TO Data_file$
250    READ #1;Xr(*),Yr(*),Rrr(*),Xx(*),Yx(*),Bbb(*)
260    ASSIGN #1 TO *
270    MASS STORAGE IS ":T15"
271    PRINT " READY :"
272    PRINT " "
280 Setkeys:  !
290    PRINT " "
300    PRINT " KEYS  #0 : INPUT S-parameters DATA "
310    PRINT "       #1 : GET S_parameters FROM tape"
320 ! PRINT "       #5 : Plotting Smith Chart as background"
330        ON KEY #0 GOTO Input_data
340        ON KEY #1 GOTO Start
350 !      ON KEY #5 GOTO Smith
360 ! !!!  ON KEY #25 GOTO Scale
370        ON KEY #24 GOTO Zr_zx
380  !     ON KEY #26 GOTO Smith1
390 ! !!!  LABEL KEY #25,"Scale"
400        LABEL KEY #24,"Z=r+jx"
410  !     LABEL KEY #26,"Scale for S21 & S12"
420 Dummy:  GOTO Dummy
430 Start0: PRINT " WRONG FILE name FOLK ! Try Again . "
440 Start:  MASS STORAGE IS ":T14"
450    PRINT "Data_file  FROM Tape ? ";
460    INPUT Data_file$
470    PRINT Data_file$
480 ! ON ERROR GOTO Start0
490    ASSIGN #1 TO Data_file$
500    READ #1;Freq_num,Freq(*),S11m(*),S11a(*),S12m(*),S12a(*),S21m(*),S21a(*),S
22a(*),S22m(*),T1$,Ids,Vds
```

```
510   ASSIGN #1 TO *
520   MASS STORAGE IS ":T15"
530   PRINT " LIST S-parameters? (Y/N) default=NO  ";
540   Ans$="N"
550   INPUT Ans$
560   PRINT Ans$
570   Lfg=0
580   IF Ans$="N" THEN Lfg=1
590   IF Lfg=1 THEN GOTO 700
600   PRINTER IS 0
610   FIXED 2
620   PRINT T1$;"   (";"Vds=";Vds;"V";" Ids=";Ids;"ma";")";" : S-parameters "
630   FIXED 3
640   PRINT " FREQ(Mhz)   S11m   S11a    S21m    S21a    S12m    S12a    S22m
 S22a "
650   FOR I=1 TO Freq_num
660   PRINT USING Image4;Freq(I),S11m(I),S11a(I),S21m(I),S21a(I),S12m(I),S12a(I)
,S22m(I),S22a(I)
670   NEXT I
680   PRINT " "
690   PRINTER IS 16
700   FOR I=1 TO Freq_num
710   IF S11a(I)<0 THEN S11a(I)=360+S11a(I)
720   IF S12a(I)<0 THEN S12a(I)=360+S12a(I)
730   IF S21a(I)<0 THEN S21a(I)=360+S21a(I)
740   IF S22a(I)<0 THEN S22a(I)=360+S22a(I)
750   NEXT I
760 List1:!
770   LOCATE 11.894273135,111.013215922,0,99.118942791
780   GRAPHICS
790   SCALE -1,1,-1,1 !!
800   PRINT "OVERLAY CURVE ? default=NO  ";
810   Ans$="N"
820   INPUT Ans$
830   PRINT Ans$
840   IF Ans$="N" THEN PLOTTER IS "GRAPHICS"
850 GOTO List
860 Int:!
870   PRINT " "
880   PRINT " Interpolation ? (Y/N)  default=NO ";
890   Ans$="N"
900   INPUT Ans$
910   PRINT Ans$
920   IF Ans$="Y" THEN GOTO Here
930   GOTO List
940 Here: PRINT " INPUT  FREQ number "
950   INPUT K1
960   PRINT K1
970   K2=K1+1
980   FOR I=Freq_num TO K2 STEP -1
990   Freq(I+1)=Freq(I)
1000  S11m(I+1)=S11m(I)
```

```
1010  S11a(I+1)=S11a(I)
1020  S21m(I+1)=S21m(I)
1030  S21a(I+1)=S21a(I)
1040  S12m(I+1)=S12m(I)
1050  S12a(I+1)=S12a(I)
1060  S22m(I+1)=S22m(I)
1070  S22a(I+1)=S22a(I)
1080  NEXT I
1090  Freq_num=Freq_num+1
1100  W2m=S11m(K2+1)
1110  W2a=S11a(K2+1)
1120  W1m=S11m(K1)
1130  W1a=S11a(K1)
1140  CALL Interp(W3m,W3a,W2m,W2a,W1m,W1a)
1150  S11m(K2)=W3m
1160  S11a(K2)=W3a
1170  W2m=S21m(K2+1)
1180  W2a=S21a(K2+1)
1190  W1m=S21m(K1)
1200  W1a=S21a(K1)
1210  CALL Interp(W3m,W3a,W2m,W2a,W1m,W1a)
1220  S21m(K2)=W3m
1230  S21a(K2)=W3a
1240  W2m=S12m(K2+1)
1250  W2a=S12a(K2+1)
1260  W1m=S12m(K1)
1270  W1a=S12a(K1)
1280  CALL Interp(W3m,W3a,W2m,W2a,W1m,W1a)
1290  S12m(K2)=W3m
1300  S12a(K2)=W3a
1310  W2m=S22m(K2+1)
1320  W2a=S22a(K2+1)
1330  W1m=S22m(K1)
1340  W1a=S22a(K1)
1350  CALL Interp(W3m,W3a,W2m,W2a,W1m,W1a)
1360  S22m(K2)=W3m
1370  S22a(K2)=W3a
1380  Freq(K2)=(Freq(K1)+Freq(K2+1))/2
1390  PRINT " LIST New S_parameters Set "
1400  PRINT " Display ON CRT (16) or Printer (0) ? ";
1410  Printer=16
1420  INPUT Printer
1430  PRINT Printer
1440  PRINTER IS Printer
1450  PRINT " FREQ(Mhz)   S11m    S11a     S21m     S21a     S12m     S12a     S22m
 S22a "
1460  FOR I=1 TO Freq_num
1470  PRINT USING Image4;Freq(I),S11m(I),S11a(I),S21m(I),S21a(I),S12m(I),S12a(I)
,S22m(I),S22a(I)
1480  NEXT I
1490  PRINTER IS 16
1500  GOTO List
```

```
1510 Listpt:!
1520  PRINT " "
1530  PRINT "   Number      S_parameter "
1540  PRINT "     1             S11      "
1550  PRINT "     2             S21      "
1560  PRINT "     3             S12      "
1570  PRINT "     4             S22      "
1580  PRINT " Number of S_parameters ? ";
1590  INPUT Num
1600  PRINT Num
1610  LOCATE 11.894273135,111.013215922,0,99.118942791
1620  GRAPHICS
1630  FIXED 0
1640  SELECT Num
1650  CASE 1
1660  SCALE -1,1,-1,1
1670    X1m=S11m(1)
1680    X1a=S11a(1)
1690    CALL Xcp(X1x,X1y,X1m,X1a)
1700    MOVE X1x,X1y
1710    LABEL "S11"
1720    MOVE X1x,X1y
1730   FOR J=2 TO Freq_num
1740    X1m=S11m(J)
1750    X1a=S11a(J)
1760    CALL Xcp(X1x,X1y,X1m,X1a)
1770    X(J)=X1x
1780    Y(J)=X1y
1790 !  PLOT X(J),Y(J)
1800    DRAW X(J),Y(J)
1810  IF J=Freq_num THEN LABEL Freq(J)
1820  NEXT J
1830  FIXED 3
1840  GOTO List
1850  CASE 2
1860  SCALE -5,5,-5,5
1870    X1m=S21m(1)
1880    X1a=S21a(1)
1890    CALL Xcp(X1x,X1y,X1m,X1a)
1900    MOVE X1x,X1y
1910    LABEL "S21"
1920    MOVE X1x,X1y
1930   FOR J=2 TO Freq_num
1940    X1m=S21m(J)
1950    X1a=S21a(J)
1960    CALL Xcp(X1x,X1y,X1m,X1a)
1970    X(J)=X1x
1980    Y(J)=X1y
1990 !  PLOT X(J),Y(J)
2000    DRAW X(J),Y(J)
```

```
2010 !  LABEL Freq(J)
2020  IF J=Freq_num THEN LABEL Freq(J)
2030  NEXT J
2040  SCALE -1,1,-1,1
2050  FIXED 3
2060  GOTO List
2070  CASE 3
2080  SCALE -.15,.15,-.15,.15
2090    X1m=S12m(1)
2100    X1a=S12a(1)
2110    CALL Xcp(X1x,X1y,X1m,X1a)
2120    MOVE X1x,X1y
2130    LABEL "S12"
2140    MOVE X1x,X1y
2150   FOR J=2 TO Freq_num
2160    X1m=S12m(J)
2170    X1a=S12a(J)
2180    CALL Xcp(X1x,X1y,X1m,X1a)
2190    X(J)=X1x
2200    Y(J)=X1y
2210 !  PLOT X(J),Y(J)
2220    DRAW X(J),Y(J)
2230 !  LABEL Freq(J)
2240  IF J=Freq_num THEN LABEL Freq(J)
2250  NEXT J
2260  SCALE -1,1,-1,1
2270  FIXED 3
2280  GOTO List
2290  CASE 4
2300    X1m=S22m(1)
2310    X1a=S22a(1)
2320    CALL Xcp(X1x,X1y,X1m,X1a)
2330    MOVE X1x,X1y
2340    LABEL "S22"
2350    MOVE X1x,X1y
2360   FOR J=2 TO Freq_num
2370    X1m=S22m(J)
2380    X1a=S22a(J)
2390    CALL Xcp(X1x,X1y,X1m,X1a)
2400    X(J)=X1x
2410    Y(J)=X1y
2420 !  PLOT X(J),Y(J)
2430    DRAW X(J),Y(J)
2440 !  LABEL Freq(J)
2450  IF J=Freq_num THEN LABEL Freq(J)
2460  NEXT J
2470  FIXED 3
2480  GOTO List
2490 Extra: Smith_set=1
2500  GOTO Smith
```

```
2510 Extra1:Smith1_set=1
2520  GOTO Smith1
2530 List:PRINT " "
2540  Smith_set=0
2550  Smith1_set=0
2560  PRINT "Number";"          FREQ(MHz)"
2570  FIXED 0
2580       PRINT "    0  ";"          Goto control "
2590  FOR Ii=1 TO Freq_num
2600  PRINT USING Image5;Ii,Freq(Ii)
2610  NEXT Ii
2620  PRINT " ";Freq_num+1;"          Interpolation S_parameters"
2630  PRINT " ";Freq_num+2;"          Goto PLOT S_parameters"
2640  PRINT " ";Freq_num+3;"          PLOT Smith Chart background"
2650  PRINT " ";Freq_num+4;"          PLOT background Scale for S21 & S12"
2660  PRINT "Number ? ";
2670  INPUT I
2680  PRINT I
2690  IF I=0 THEN GOTO Setkeys
2700  IF I=Freq_num+1 THEN GOTO Int
2710  IF I=Freq_num+2 THEN GOTO Listpt
2720  IF I=Freq_num+3 THEN GOTO Extra
2730  IF I=Freq_num+4 THEN GOTO Extra1
2740  IF I>Freq_num THEN GOTO Listpt
2750  PRINT I;" FREQ = ";
2760  FIXED 3
2770  PRINT Freq(I);"MHz";
2780  Freq=Freq(I)
2790  S11m=S11m(I)
2800  S11a=S11a(I)
2810  S12m=S12m(I)
2820  S12a=S12a(I)
2830  S21m=S21m(I)
2840  S21a=S21a(I)
2850  S22m=S22m(I)
2860  S22a=S22a(I)
2870  CALL Xcp(S11x,S11y,S11m,S11a)
2880  CALL Xcp(S12x,S12y,S12m,S12a)
2890  CALL Xcp(S21x,S21y,S21m,S21a)
2900  CALL Xcp(S22x,S22y,S22m,S22a)
2910  CALL Mcp(S1122x,S1122y,S11x,S11y,S22x,S22y)
2920  CALL Mcp(S1221x,S1221y,S12x,S12y,S21x,S21y)
2930  Deltax=S1122x-S1221x
2940  Deltay=S1122y-S1221y
2950  Sqdel=Deltax*Deltax+Deltay*Deltay
2960  Sqs22=S22x*S22x+S22y*S22y
2970  Sqs11=S11x*S11x+S11y*S11y
2980  Sqs21=S21x*S21x+S21y*S21y
2990  Sqs12=S12x*S12x+S12y*S12y
3000  Sqs1221=S1221x*S1221x+S1221y*S1221y
```

```
3010  Mods1221=SQR(Sqs1221)
3020  D2=Sqs22-Sqdel
3030  D1=Sqs11-Sqdel
3040  CALL Mcp(Ds22cx,Ds22cy,Deltax,Deltay,S22x,-S22y)
3050  C1x=S11x-Ds22cx
3060  C1y=S11y-Ds22cy
3070  B1=1+Sqs11-Sqs22-Sqdel
3080  CALL Mcp(Ds11cx,Ds11cy,Deltax,Deltay,S11x,-S11y)
3090  C2x=S22x-Ds11cx
3100  C2y=S22y-Ds11cy
3110  B2=1+Sqs22-Sqs11-Sqdel
3120  Yy=2*Mods1221
3130  K=(1+Sqdel-Sqs11-Sqs22)/Yy
3140  PRINT "  Stability factor = ";K
3150  IF K<1 THEN PRINT "   NO Gmax !"
3160  Sqmsg=Sqs21/Sqs12
3170  Mods21d12=SQR(Sqmsg)
3180  Sqc1=C1x*C1x+C1y*C1y
3190  Sqc2=C2x*C2x+C2y*C2y
3200  Modc1=SQR(Sqc1)
3210  Modc2=SQR(Sqc2)
3220  Sq11del=Sqs11-Sqdel
3230  Sq22del=Sqs22-Sqdel
3240  Rs1x=C1x/Sq11del
3250  Rs1y=-C1y/Sq11del
3260  Rs2x=C2x/Sq22del
3270  Rs2y=-C2y/Sq22del
3280  Rads=Mods1221/Sq11del
3290  Radl=Mods1221/Sq22del
3300  Rs1mod=SQR(Rs1x^2+Rs1y^2)
3310  Rs2mod=SQR(Rs2x^2+Rs2y^2)
3320  CALL Rcp(C1mag,C1ang,Rs2x,Rs2y)
3330  CALL Rcp(Csmag,Csang,Rs1x,Rs1y)
3340   Rads=ABS(Rads)
3350   Radl=ABS(Radl)
3360   Msg=10*LGT(Mods21d12)
3370  IF K<1 THEN
3380      IF Rs2mod-Radl>0 THEN S1$="OUTSIDE circle"  !(A)O/P
3390      IF Rs2mod-Radl<=0 THEN S1$=" INSIDE circle"  !(B)O/P
3400      FIXED 10
3410      PRINT "  RR";Rs2mod-Radl
3420      FIXED 3
3430      IF Rs1mod-Rads>0 THEN Ss$="OUTSIDE circle"   !(A)I/P
3440      IF Rs1mod-Rads<0 THEN Ss$=" INSIDE circle"  !(B)I/P
3450  ELSE
3460      IF Rs2mod<1 THEN
3470           IF (Rs2mod>Radl) AND (2*Radl<1) THEN S1$="OUTSIDE circle"!(C)O/P
3480      ELSE
3490           IF (Rs2mod<Radl) AND (Radl<1) THEN S1$=" INSIDE circle"!(D)O/P
3500      END IF
```

```
3510       IF (Rs2mod-1)=Rad1) AND (Rs2mod)1) THEN S1$="UNCONDITION    "!(E)O/P
3520       IF Rad1)1+Rs2mod THEN S1$="UNCONDITION    " !(F)O/P
3530       IF Rs1mod<1 THEN
3540            IF (Rs1mod)Rads) AND (2*Rads<1) THEN Ss$="OUTSIDE circle"!(C)I/P
3550       ELSE
3560            IF (Rs1mod<Rads) AND (Rads<1) THEN Ss$=" INSIDE circle"!(D)I/P
3570       END IF
3580       IF (Rs1mod-1)=Rads) AND (Rs1mod)1) THEN Ss$="UNCONDITION    "!(E)I/P
3590       IF Rads)1+Rs1mod THEN Ss$="UNCONDITION    " !(F)I/P
3600  END IF
3610  PRINT " PRINT Tittle ? (Y/N)  default is NO ";
3620  INPUT Ans$
3630  PRINT Ans$
3640  IF Ans$="N" THEN Flag=1
3650  PRINT " PRINTER IS CRT/HARD COPY ? CRT=16 ;COPY =0  default=16 "
3660  Printer=16
3670  INPUT Printer
3680  PRINT Printer
3690  PRINTER IS Printer
3700  IF Ans$="N" THEN GOTO 3730
3710  FIXED 2
3720  PRINT T1$;"    (";"Vds=";Vds;"V";" Ids=";Ids;"ma";")"
3730  FIXED 3
3740  PRINT "                                                STABILITY CIRCLE     "
3750  PRINT "                                      INPUT PLANE                OUTPUT PLANE"
3760  PRINT "                              Origin          Radius       Origin          Rad
ius"
3770  PRINT "FREQ(Mhz)     K         CSmag    CSang     Rads       CLmag    CLang     R
ad1"
3780  PRINT USING Image1;Freq;K;Csmag;Csang;Rads;Clmag;Clang;Rad1
3790  PRINT " "
3800  PRINT " STABILITY region:      ";Ss$;"                  ";S1$
3810  PRINT " "
3820  PRINT "Rs1mod/Rs1:";Rs1mod;"/";Rads;";Rs2mod/Rs2:";Rs2mod;"/";Rad1;"; MSG
=";Msg;"dB"
3830  PRINT " "
3840  PRINTER IS 16
3850  Cxxx(2)=Rs2x
3860  Cyyy(2)=Rs2y
3870  Rmodd(2)=Rad1
3880  Cxxx(1)=Rs1x
3890  Cyyy(1)=Rs1y
3900  Rmodd(1)=Rads
3910  PRINT " PLOT Stability circle ? (Y/N) default=YES  ";
3920  Ans$="Y"
3930  INPUT Ans$
3940  PRINT Ans$
3950  IF Ans$="N" THEN GOTO Listno
3960  PRINT " ON which plane ?(INPUT plane=1 OR OUTPUT plane=2) default=2 ";
3970  Jj=2
3980  INPUT Jj
3990  PRINT Jj
4000  Cxx=Cxxx(Jj)
```

```
4010  Cyy=Cyyy(Jj)
4020  Rmod=Rmodd(Jj)
4030  PRINT " FILL CIRCLE ? YES =1 NO = 0  ";
4040  Flg=0
4050  INPUT Flg
4060  PRINT Flg
4070  PRINT " Erase ?   Y=1 N=0 default NO ";
4080  Flge=0
4090  INPUT Flge
4100  PRINT Flge
4110  CALL Plot(Rmod,Cxx,Cyy,Flg,Flge)
4120  Flg=0
4130  ! GAIN ONLY FOR K>1 or K = 1
4140 Listno: !
4150  IF K*K-1<0 THEN GOTO Continue
4160  Kk=SQR(K*K-1)
4170  IF B1<0 THEN Kkk=K+Kk
4180  IF B1>0 THEN Kkk=K-Kk
4190  Gmax=Mods21d12*Kkk
4200  G=10*LGT(Gmax)
4210  Xx=SQR(B1*B1-4*Sqc1)
4220  IF B1<0 THEN Xxx=B1+Xx
4230  IF B1>0 THEN Xxx=B1-Xx
4240  Xxxx=Xxx/Sqc1
4250  X=Xxxx/2
4260  Rmsx=C1x*X
4270  Rmsy=-C1y*X
4280  Xx=SQR(B2*B2-4*Sqc2)
4290  IF B2<0 THEN Xxx=B2+Xx
4300  IF B2>0 THEN Xxx=B2-Xx
4310  Xxxx=Xxx/Sqc2
4320  X=Xxxx/2
4330  Rmlx=C2x*X
4340  Rmly=-C2y*X
4350  CALL Rcp(Rmlm,Rmla,Rmlx,Rmly)
4360  CALL Rcp(Rmsm,Rmsa,Rmsx,Rmsy)
4370  PRINTER IS Printer
4380  PRINT "SIMULTANEOUS MATCH FOR MAXIMUM GAIN"
4390  PRINT "FREQ(MHz)   Gmax     Input match Imp.  Output match Imp. "
4400  PRINT "            (dB)      ZSmag  ZSang        ZLmag ZLang      "
4410  PRINT USING Image2;Freq;G;Rmsm;Rmsa;Rmlm;Rmla
4411  PRINT " "
4420  CALL Ratorx(Msource_r,Msource_x,Rmsm,Rmsa)
4430  PRINT "INmatch-r=";Msource_r;"INmatch-x=";Msource_x;
4440  CALL Ratorx(Mload_r,Mload_x,Rmlm,Rmla)
4450  PRINT "  OUTmatch-r=";Mload_r;" OUTmatch-x=";Mload_x
4460  PRINT " In 50 Ohms System : (Resistor in Ohms)"
4470  Msource_r50=ABS(Msource_r*50)
4480  Mload_r50=ABS(Mload_r*50)
4490  Tpf=2*PI*Freq
4500  IF Msource_x<0 THEN
```

```
4510   Msource_cap=ABS(1000000/(Tpf*Msource_x*50))
4520   PRINT " INmatch-R=";Msource_r50;" INmatch-CAP(pF)=";Msource_cap;
4530   ELSE
4540   Msource_ind=ABS(Msource_x*50*1000/Tpf)
4550   PRINT " INmatch-R=";Msource_r50;" INmatch-IND(nH)=";Msource_ind;
4560   END IF
4570  IF Mload_x<0 THEN
4580   Mload_cap=ABS(1000000/(Tpf*Mload_x*50))
4590   PRINT " OUTmatch-R=";Mload_r50;" OUTmatch-CAP(pF)=";Mload_cap
4600   ELSE
4610   Mload_ind=ABS(Mload_x*50*1000/Tpf)
4620   PRINT " OUTmatch-R=";Mload_r50;" OUTmatch-IND(nH)=";Mload_ind
4621   PRINT " "
4630   END IF
4640   !
4650  CALL Ratorx(Source_r,Source_x,Rmsm,360-Rmsa)
4660  PRINT "Source-r=";Source_r;" Source-x=";Source_x;
4670  CALL Ratorx(Load_r,Load_x,Rmlm,360-Rmla)
4680  PRINT "     Load-r=";Load_r;" Load-x=";Load_x
4690  PRINT " In 50 Ohms System : (Resistor in Ohms)"
4700  Source_r50=ABS(Source_r*50)
4710  Load_r50=ABS(Load_r*50)
4720  IF Source_x<0 THEN
4730   Source_cap=ABS(1000000/(Tpf*Source_x*50))
4740   PRINT "SE: Source-R=";Source_r50;" Source-CAP(pF)=";Source_cap
4741   Source_rp50=Source_r50*(1+(Source_x/Source_r)^2)
4742   X_capp=Source_r*Source_rp50/Source_x
4743   Source_capp=ABS(1000000/(Tpf*X_capp))
4744   PRINT "PA: Source-R=";Source_rp50;" Source-CAP(pF)=";Source_capp
4750   ELSE
4760   Source_ind=ABS(Source_x*50*1000/Tpf)
4770   PRINT "SE: Source-R=";Source_r50;" Source-IND(nH)=";Source_ind
4771   Source_rp50=Source_r50*(1+(Source_x/Source_r)^2)
4772   X_ind=Source_r*Source_rp50/Source_x
4773   Source_indp=ABS(X_ind*1000/Tpf)
4774   PRINT "PA: Source-R=";Source_rp50;" Source-IND(nH)=";Source_indp
4780   END IF
4790  IF Load_x<0 THEN
4800   Load_cap=ABS(1000000/(Tpf*Load_x*50))
4810   PRINT "SE: Load-R=";Load_r50;" Load-CAP(pF)=";Load_cap
4811   Load_rp50=Load_r50*(1+(Load_x/Load_r)^2)
4812   Xl_capp=Load_r*Load_r50/Load_x
4813   Load_capp=ABS(1000000/(Tpf*Xl_capp))
4814   PRINT "PA: Load-R=";Load_rp50;" Load-CAP(pF)=";Load_capp
4820   ELSE
4830   Load_ind=ABS(Load_x*50*1000/Tpf)
4840   PRINT "SE: Load-R=";Load_r50;" Load-IND(nH)=";Load_ind
4841   Load_rp50=Load_r50*(1+(Load_x/Load_r)^2)
4842   Xl_ind=Load_r*Load_r50/Load_r
4843   Load_indp=ABS(Xl_ind*1000/Tpf)
4844   PRINT "PA: Load-R=";Load_rp50;" Load-IND(nH)=";Load_indp
4850   END IF
4860  !
4870  PRINT " "
4880  PRINTER IS 16
4890  Gg=G
4900  GOTO Call
```

```
4910 Continue: Gg=100! Dummy gain for K<1
4920 Call: ! Constant gain circle for giving gain in dB
4930  PRINT " "
4940  PRINT " PLOT desired constant GAIN CIRCLE?(Y/N) default=NO ";
4950  Ans$="N"
4960  INPUT Ans$
4970  PRINT Ans$
4980  IF Ans$="N" THEN GOTO List
4990 Agn:PRINT " Desired GAIN (dB) ? = ";
5000  INPUT Mm
5010  PRINT Mm
5020  PRINT " "
5030  PRINT " Input plane = 1 OR output plane = 2 ? default = 2 ";
5040  Ss=2
5050  INPUT Ss
5060  PRINT Ss
5070  IF Ss=1 THEN Sse_flag=1
5080  IF Ss=2 THEN Sse_flag=0
5090  IF Gg-Mm<0 THEN GOTO Next
5100  Gm=10^(Mm/10)
5110  Gm=Gm/Sqs21
5120  G=Mm
5130  IF Sse_flag=1 THEN GOTO Source0
5140  ! LOAD
5150  Co20=Gm/(1+D2*Gm)
5160  ! CO2 : Center of the constant gain circle on the o/p plane
5170  Co2x=C2x*Co20
5180  Co2y=-C2y*Co20
5190  GOTO 5260
5200  ! SOURCE
5210 Source0:!
5220  Co20=Gm/(1+D1*Gm)
5230  Co2x=C1x*Co20
5240  Co2y=-C1y*Co20
5250  D2=D1
5260  Sqs1221gm=Sqs1221*Gm*Gm
5270  Mods1221gm=SQR(Sqs1221gm)
5280  Ro2=SQR(1-2*K*Mods1221gm+Sqs1221gm)
5290  Ro2=Ro2/(1+D2*Gm)
5300  CALL Rcp(Co2mag,Co2ang,Co2x,Co2y)
5310  Rmlxx=Co2x
5320  Rmlyy=Co2y
5330  CALL Rcp(Rmlmag,Rmlang,Rmlxx,Rmlyy)
5340  PRINT " FILL CIRCLE ? YES=1;NO=0  ";
5350  INPUT Flg
5360  PRINT Flg
5370  PRINT "Plot";Mm;"dB Constant gain circle ....."
5380  FIXED 1
5390  Ans$="N"
5400  PRINT "Erase Curve ? Y=1 N=0 default NO ";
5410  Flge=0
5420  INPUT Flge
5430  PRINT Flge
5440  CALL Plot(Ro2,Co2x,Co2y,Flg,Flge)
5450  Flge=0
5460  Flg=0
5470  PRINT " LABEL ' Gain dB Circle ' (Y/N)  default=NO ";
5480  INPUT Ans$
5490  PRINT Ans$
5500  IF Ans$="N" THEN GOTO Coctll
5510  LORG 2
5520  MOVE Rmlxx,Rmlyy
```

```
5530  LABEL Mm;"dB Circle"
5540  LORG 1
5550 Coct11:PRINT "Plot OK! Press 'CONT' NOW"
5560  PAUSE    ! Rms
5570  PRINT "Pick Load Impedance ? (Y/N) default=NO  ";
5580  Ans$="N"
5590  INPUT Ans$
5600  PRINT Ans$
5610  IF Ans$="N" THEN GOTO Cont1
5620  PRINT " resistance = ";
5630  INPUT Zr
5640  PRINT Zr
5650  PRINT " susceptance = ";
5660  INPUT Zx
5670  PRINT Zx
5680  CALL Zrtorho(Rhox,Rhoy,Zr,Zx)
5690  CALL Mcp(R2delx,R2dely,Rhox,Rhoy,Deltax,Deltay)!r2*DELTA
5700  IF Sse_flag=1 THEN GOTO Source1
5710  CALL Mcp(R2s22x,R2s22y,Rhox,Rhoy,S22x,S22y)!r1*S22
5720  Ax=S11x-R2delx
5730  By=S11y-R2dely
5740  Cx=1-R2s22x
5750  Dy=-R2s22y
5760  GOTO 5830
5770 Source1: !

5780  CALL Mcp(R2s11x,R2s11y,Rhox,Rhoy,S11x,S11y)!r1*S11
5790  Ax=S22x-R2delx
5800  By=S22y-R2dely
5810  Cx=1-R2s11x
5820  Dy=-R2s11y
5830  CALL Dcp(Pickx,Picky,Ax,By,Cx,Dy)
5840  Picky=-Picky
5850  CALL Rcp(Rmsmag,Rmsang,Pickx,Picky)
5860   LORG 2
5870   MOVE Pickx,Picky
5880   LABEL "# rms"
5890   LORG 1
5900 Cont1:PRINT " Plot more circle ? (Y/N) default=NO ";
5910  Ans$="N"
5920  INPUT Ans$
5930  PRINT Ans$
5940  IF Ans$="Y" THEN GOTO Agn
5950 Next:FIXED 3
5960  IF K<1 THEN GOTO List
5970  PRINT " LABEL ZLmax & ZSmax ? (Y/N) defaut NO ";
5980  Ans$="N"
5990  INPUT Ans$
6000  PRINT Ans$
6010  IF Ans$="N" THEN GOTO List
6020  LORG 2
6030  MOVE Rmlx,Rmly
6040  LABEL "* ZLmax"
6050  MOVE Rmsx,Rmsy
6060  LABEL "* ZSmax"
6070  LORG 1 !
6080  GOTO List
```

```
6090 Smith: !
6100  SHORT Xr(6,204),Yr(6,204),A(20,204)
6110  SHORT Xx(10,102),Yx(10,102)
6120  SHORT Ctr(20),Ctx(20),Rrr(20),Bbb(20),Ct(20)
6130  Nrr=6
6140  Nxx=10
6150  PRINT "Overlay previous PLOT? Y/N ? default= Yes  ";
6160  Ans$="Y"
6170  INPUT Ans$
6180  PRINT Ans$
6190  IF Ans$="N" THEN PLOTTER IS "GRAPHICS"
6200  GRAPHICS
6210  LOCATE 11.894273135,111.013215922,0,99.118942791
6220  SCALE -1,1,-1,1
6230 ! Data_file$="S2"
6240 ! ASSIGN #1 TO Data_file$
6250 ! READ #1;Xr(*),Yr(*),Rrr(*),Xx(*),Yx(*),Bbb(*)
6260 ! ASSIGN #1 TO *
6270  GOTO Sun
6280  DATA 0,0.2,0.5,1,2,5
6290  DATA .2,-.2,.5,-.5,1,-1,2,-2,5,-5
6300  FOR J=1 TO 6
6310  READ Rrr(J)
6320  Ct(J)=1/(Rrr(J)+1)
6330  X=1-Ct(J)
6340  Y=0
6350  MOVE X,Y
6360  POLYGON Ct(J),360
6370  NEXT J
6380  FOR I=1 TO 10
6390  READ Bbb(I)
6400  X=1
6410  Y=1/Bbb(I)
6420  MOVE X,Y
6430  POLYGON Y,360
6440  NEXT I
6450  GOTO Subend1
6460 Sun:Erase=0
6470 ! Plot
6480  PRINT " Erase Curve ? Y=1 N=0 ";
6490  INPUT Erase
6500  PRINT Erase
6510  IF Erase=1 THEN PEN -1
6520  IF Erase=0 THEN PEN 1
6530  FIXED 1
6540  LINE TYPE 3
6550  IF Erase=1 THEN LINE TYPE 1
6560 FOR J=1 TO Nrr
6570  MOVE Xr(J,1),Yr(J,1)
6580  FOR I=1 TO 204
6590  DRAW Xr(J,I),Yr(J,I)
6600  NEXT I
6610  MOVE Xr(J,102),0
6620  CSIZE 2
6630  LINE TYPE 1
6640  LABEL Rrr(J)
6650  LINE TYPE 3
6660  IF Erase=1 THEN LINE TYPE 1
6670  NEXT J
```

```
6680  ! Draw center line
6690  MOVE 1,0
6700  DRAW -1,0
6710 FOR J=1 TO Nxx
6720  MOVE Xx(J,1),Yx(J,1)
6730  SELECT J
6740  CASE 1
6750  Nn=15
6760  CASE 2
6770  Nn=15
6780  CASE 3
6790  Nn=32
6800  CASE 4
6810  Nn=32
6820  CASE 5
6830  Nn=51
6840  CASE 6
6850  Nn=51
6860  CASE 7
6870  Nn=73
6880  CASE 8
6890  Nn=73
6900  CASE 9
6910  Nn=90
6920  CASE ELSE
6930  Nn=90
6940  END SELECT
6950  FOR I=1 TO Nn
6960  LINE TYPE 3
6970  IF Erase=1 THEN LINE TYPE 1
6980  DRAW Xx(J,I),Yx(J,I)
6990  NEXT I
7000  LINE TYPE 1
7010  LABEL Bbb(J)
7020  NEXT J
7030  FIXED 3
7040  END SELECT
7050 Subend1: PRINT "  "
7060  PRINT "PLOT ? default=Yes  ";
7070  Ans$="Y"
7080  INPUT Ans$
7090  PRINT Ans$
7100   IF Ans$="N" THEN EXIT GRAPHICS
7110   IF Ans$="Y" THEN DUMP GRAPHICS
7120   PRINT "TERMINATE ? (Y/N) default=No ";
7130   Ans$="N"
7140   INPUT Ans$
7150   PRINT Ans$
7160   IF Ans$="N" THEN GOTO List1
7170   IF (Smith_set=1) AND (Ans$="N") THEN GOTO List1
7180  GOTO Terminate
7190 Smith1: !
7200  LOCATE 11.894273135,111.013215922,0,99.118942791
7210  GRAPHICS
7220  SCALE -5,5,-5,5
7230  DEG
7240  LINE TYPE 3
7250  FOR I=1 TO 5
7260  MOVE 0,0
7270  POLYGON I,360
7280  NEXT I
7290  FOR I=1 TO 12
```

```
7300  MOVE 0,0
7310  LDIR I*30
7320  LINE TYPE 3
7330  DRAW 5*COS(I*30),5*SIN(I*30)
7340  LINE TYPE 1
7350  LABEL I*30
7360  NEXT I
7370  CSIZE 2
7380  MOVE 0,0
7390  FOR I=1 TO 5
7400  MOVE 0,-I
7410  LABEL I
7420  NEXT I
7430  FIXED 3
7440  MOVE 0,0
7450  FOR I=1 TO 5
7460  MOVE I,-.3
7470  LABEL .03*I
7480  NEXT I
7490  MOVE .1,-4.5
7500  LABEL "S21"
7510  MOVE 5.3,-.6
7520  LABEL "S12"
7530  IF Smith1_set=1 THEN GOTO Subend1
7540  GOTO Setkeys
7550 Zr_zx: !
7560  LOCATE 11.894273135,111.013215922,0,99.118942791
7570  SCALE -1,1,-1,1
7580  GRAPHICS
7590  DIM Rorx$[3]
7600  PRINT "PLOT r or X : (R/X) ? ";
7610  INPUT Rorx$
7620  PRINT Rorx$
7630  IF Rorx$="R" THEN
7640  PRINT "r=?";
7650  INPUT Rrr
7660  PRINT Rrr
7670  Ct=1/(Rrr+1)
7680  ELSE
7690  IF Rorx$<>"X" THEN GOTO 7600
7700  PRINT "x=? ";
7710  INPUT Zx
7720  PRINT Zx
7730  Ct=1/Zx
7740  END IF
7750  IF Rorx$="R" THEN
7760  X=1-Ct
7770  Y=0
7780  ELSE
7790  X=1
7800  Y=Ct
7810  END IF
7820  MOVE X,Y
7830  PRINT " Erase CURVE ? Yes=1;NO=0 default NO";
7840  Flge=0
7850  INPUT Flge
7860  PRINT Flge
```

```
7870  IF Flge=1 THEN PEN -1
7880  IF Flge=0 THEN PEN 1
7890  POLYGON Ct,360
7900  GOTO Setkeys
7910  !
7920 Input_data:!
7930  PRINT " DEVICE NAME = ";
7940  INPUT T1$
7950  PRINT T1$
7960  PRINT " Vds (V) = ";
7970  INPUT Vds
7980  PRINT Vds
7990  PRINT " Ids (ma) = ";
8000  INPUT Ids
8010  PRINT Ids
8020  PRINT " Number of Frequency = ";
8030  INPUT Freq_num
8040  PRINT Freq_num
8050  PRINT " FREQ(MHz)   S11m    S11a     S21m     S21a     S12m     S12a      S22m
 S22a"
8060  FOR I=1 TO Freq_num
8070 Repeat:Ans$="Y"
8080  INPUT Freq(I),S11m(I),S11a(I),S21m(I),S21a(I),S12m(I),S12a(I),S22m(I),S22a
(I)
8090  PRINT USING Image4;Freq(I),S11m(I),S11a(I),S21m(I),S21a(I),S12m(I),S12a(I)
,S22m(I),S22a(I)
8100  PRINT " OK ? (Y/N) :";
8110  INPUT Ans$
8120  PRINT Ans$
8130  IF Ans$="Y" THEN
8140  GOTO Ok
8150  ELSE
8160  PRINT "Repeat Again !"
8170  GOTO Repeat
8180  END IF
8190 Ok:NEXT I
8200  PRINT "Data_file$ ?";
8210  INPUT Data_file$
8220  PRINT Data_file$
8230  MASS STORAGE IS ":T14"
8240  CREATE Data_file$,3
8250  ASSIGN #1 TO Data_file$
8260  PRINT #1;Freq_num,Freq(*),S11m(*),S11a(*),S12m(*),S12a(*),S21m(*),S21a(*),
S22a(*),S22m(*),T1$,Ids,Vds
8270  ASSIGN #1 TO *
8280  MASS STORAGE IS ":T15"
8290  GOTO Setkeys
8300 Scale:  ALPHA
8310 ! FIXED 1
8320 Cont:GRAPHICS INPUT IS "ARROW KEYS"
8330  POINTER 0,0,2
8340  GRAPHICS
8350  FIXED 9
8360  DIGITIZE X1,Y1
8370  PRINT X,Y
8380  PRINT " FOR S11 & S22 (1) ; FOR S21 (2) ;FOR S12 (3) ? default =1 ";
8390   Ssnum=1
8400   INPUT Ssnum
8410   PRINT Ssnum
8420   IF Ssnum=1 THEN Two=2
8430   IF Ssnum=2 THEN Two=10
8440   IF Ssnum=3 THEN Two=.3
8450  X0001=11.894273135+111.013215922
8460  X0002=111.013215922-11.894273135
```

```
8470  X0=X0001/2
8480  Y0=99.118942791/2
8490  X0rad=X0002/Two
8500  Y0rad=99.118942791/Two
8510  PRINT "X0001=";X0001;"X0002=";X0002;"X0=";X0;"Y0=";Y0;"X0rad=";X0rad;"Y0ra
d";Y0rad
8520  Xloc=(X-X0)/X0rad
8530  Yloc=(Y-Y0)/Y0rad
8540  PRINT "Xloc=";Xloc;" Yloc=";Yloc
8550  CALL Rcp(Rhomag,Rhoang,Xloc,Yloc)
8560  PRINT "Rhomag=";Rhomag;" Rhoang=";Rhoang
8570  IF (Ssnum=2) OR (Ssnum=3) THEN GOTO Cont11
8580  CALL Rhotozr(Zr,Zx,Xloc,Yloc)
8590  PRINT "Zr=";Zr;" Zx=";Zx
8600 ! CALL Rhotogg(Gg,Gb,Xloc,Yloc)
8610 ! PRINT "Gg=";Gg;" Gb=";Gb
8620  PRINT " "
8630 Cont11:PRINT " More Scaling ? ";
8640  Ans$="Y"
8650  INPUT Ans$
8660  PRINT Ans$
8670  IF Ans$="Y" THEN GOTO Cont
8680  GOTO Setkeys
8690 Terminate: OFF KEY #0
8700            OFF KEY #1
8710            OFF KEY #2
8720            OFF KEY #3
8730            OFF KEY #5
8740            OFF KEY #24
8750            OFF KEY #25
8760      LABEL KEY #24," "
8770      LABEL KEY #25," "
8780      LABEL KEY #26," "
8790  STOP
8800  END
8810  !
8820  SUB Mcp(X,Y,A,B,C,D)
8830  X=A*C-B*D
8840  Y=A*D+B*C
8850  SUBEND
8860  SUB Dcp(X,Y,A,B,C,D)
8870  Z=C*C+D*D
8880  X=(A*C+B*D)/Z
8890  Y=(B*C-A*D)/Z
8900  SUBEND
8910  !
8920  SUB Rcp(R,A,X,Y)
8930  DEG
8940  R=SQR(X*X+Y*Y)
8950  A=ATN(Y/X)
8960  IF X<0 THEN A=A+180
8970  IF (X>0) AND (Y<0) THEN A=A+360
8980  SUBEND
8990  !
9000  SUB Xcp(X,Y,R,A)
9010  DEG
9020  X=R*COS(A)
9030  Y=R*SIN(A)
9040  SUBEND
9050  SUB Plot(Radius,Centerx,Centery,Flg,Flge)
```

```
9060  SHORT Xxr(104),Yyr(104)
9070  DEG
9080   GRAPHICS
9090  LOCATE 11.894273135,111.013215922,0,99.118942791
9100   SCALE -1,1,-1,1
9110   IF Flge=0 THEN PEN 1
9120   IF Flge=1 THEN PEN -1
9130   MOVE Centerx,Centery
9140   IF Flg=0 THEN GOTO 9180
9150   AREA INTENSITY RND*1,0,0
9160   POLYGON Radius,360,FILL
9170   GOTO Endsub
9180   POLYGON Radius,360
9190   GOTO Endsub
9200   St=360/103
9210   FOR J=1 TO 104
9220   A=-St+J*St
9230   CALL Xcp(X,Y,Radius,A)
9240   Xxr(J)=X+Centerx
9250   Yyr(J)=Y+Centery
9260   NEXT J
9270  MOVE Xxr(1),Yyr(1)
9280  FOR J=1 TO 104
9290  DRAW Xxr(J),Yyr(J)
9300  NEXT J
9310 Endsub: SUBEND
9320  SUB Zrtorho(Rhox,Rhoy,Zr,Zx)
9330  Zrp=Zr+1
9340  Zrm=Zr-1
9350  CALL Dcp(Rhox,Rhoy,Zrm,Zx,Zrp,Zx)
9360  SUBEND
9370  SUB Interp(W3m,W3a,W2m,W2a,W1m,W1a)
9380  DEG
9390  CALL Xcp(W2x,W2y,W2m,W2a)
9400  CALL Xcp(W1x,W1y,W1m,W1a)
9410  W3x=(W2x+W1x)/2
9420 ! W3y=(W2y+W1y)/2
9430  Hh=(W2y+W1y)/2
9440  R=(Wx3-W1x)/2
9450  Dely=W2y-W1y
9460 ! W3y=Hh+R*(R-1)*Dely*Dely/2
9470  Ex=R*(R+2)*(R+1)*Dely^3
9480  Ex=Ex/(3*2)
9490  W3y=Hh+R*(R+1)*Dely*Dely/2+Ex
9500  CALL Rcp(W3m,W3a,W3x,W3y)
9510  SUBEND
9520  SUB Rhotozr(Zr,Zx,Rhox,Rhoy)
9530  DEG
9540  Rhop=1+Rhox
```

```
9550  Rhom=1-Rhox
9560  CALL Dcp(Zr,Zx,Rhop,Rhoy,Rhom,-Rhoy)
9570  SUBEND
9580  SUB Zrtogg(Gg,Gb,Zr,Zx)
9590  Den=Zr*Zr+Zx*Zx
9600  Gg=Zr/Den
9610  Gb=-Zx/Den
9620  SUBEND
9630  SUB Ggtozr(Zr,Zx,Gg,Gb)
9640  Den=Gg*Gg+Gb*Gb
9650  Zr=Gg/Den
9660  Zx=-Gb/Den
9670  SUBEND
9680  SUB Rhotogg(Gg,Gb,Rhox,Rhoy)
9690  Rhom=1-Rhox
9700  Rhop=1+Rhox
9710  CALL Dcp(Gg,Gb,Rhom,-Rhoy,Rhop,Rhoy)
9720  SUBEND
9730  SUB Ratorx(Zr,Zx,R,A)
9740  CALL Xcp(X,Y,R,A)
9750  CALL Rhotozr(Zr,Zx,X,Y)
9760  SUBEND
```

CHAPTER 4 DESIGN PRINCIPLES FOR POWER AMPLIFIERS

4.1 Biasing FETs for Optimum Performance.

The GaAs FETs are typically unconditionally stable within the frequency range at which they are designed to work, but outside the frequency band of interest, they are conditionally stable, i.e., their stability is determined by the source and/or load impedances presented to it. The unstable regions can be plotted on the Smith chart, which has been described in Chapter 3, using the S-parameters of the device. Typical plot of such regions are shown in Figure 4.1.1 for input plane and Figure 4.1.2 for output plane of the NE72089. The instability at high frequencies do not pose much of a problem because of the low gain of the device and relatively small unstable regions. Careful examination of the Figure 4.1.2 shows that the unstable regions become larger and extend towards the center of the Smith chart with decreasing frequency. These unstable regions can be significantly different in their magnitude and phase on the Smith chart for different devices, therefore it is desirable to develop a circuit which will provide the low frequency stabilization to any GaAs FET in general.

In principle, one has to avoid any source and load impedances that might lie within the corresponding unstable region. In practice, source and load impedances are the resultant impedances of the bias network and the matching network.

In most cases, the matching networks are of the low pass prototype(1), unless it has low frequency poles. The input impedance plot on the Smith chart with termination of 50 ohm load will spiral into the center of the chart with decreasing frequency, providing an adequate match to keep the device stable, therefore if the bias network is developed to ensure that it presents a good 50 ohm match and low insertion loss in the operating frequency band so that it does not

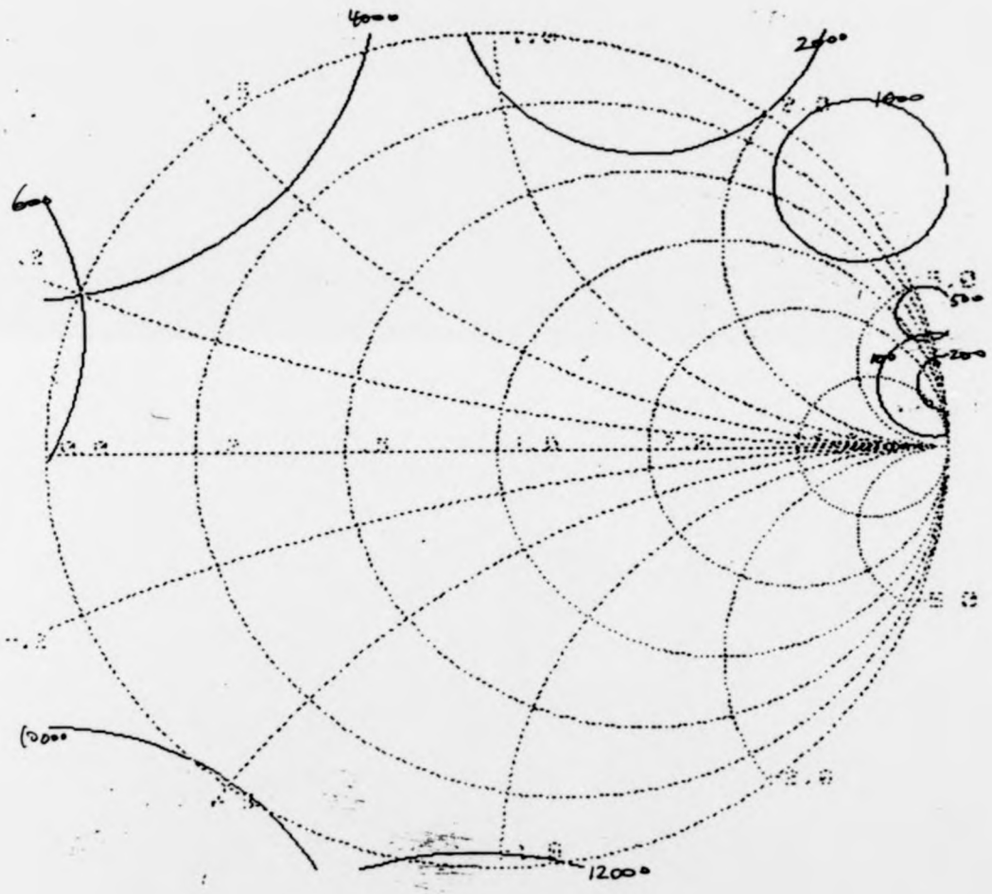


Figure 4.1.1 The Unstable Impedance Region on the Input Plane of the NE72089
(From 100 MHz to 12000 MHz)

STABILITY CIRCLE

FREQ(Mhz)	K	INPUT PLANE Origin CSmag	CSang	Radius Rads	OUTPUT PLANE Origin CLmag	CLang	Radius Radl
12000.00	.89	2.14	264.94	1.20	1.87	218.76	.92
STABILITY region:		OUTSIDE circle			OUTSIDE circle		

Rslmod/Rsl: 2.139 / 1.199 ;Rs2mod/Rs2: 1.869 / .922 ; MSG = 10.594 dB

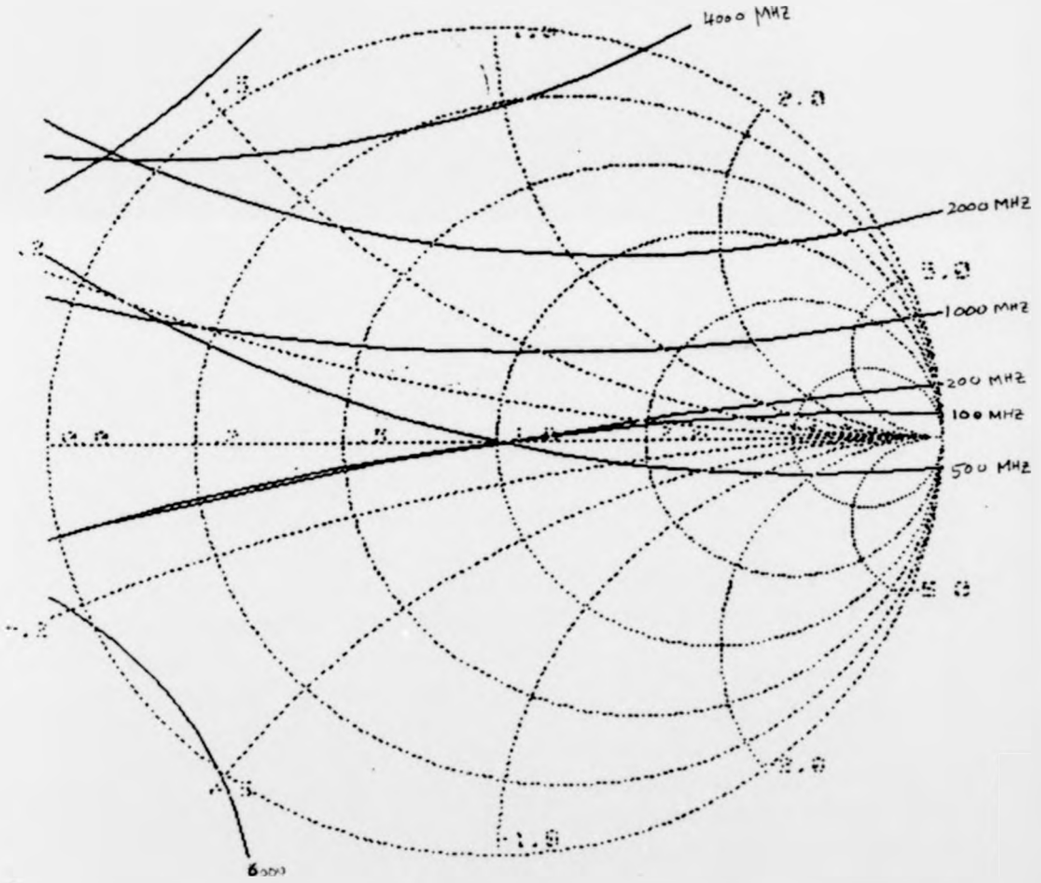


Figure 4.1.2 The Unstable Impedance Region on the Output Plane of the NE72089 (From 100 MHz to 4000 MHz)

affect the response of the matching circuits, also, it presents a good 50 ohm match and hign insertion loss at low frequencies to the device. If the low frequency behaviour of the matching network is not adequate to keep the device stable then one may insert the bias network between the matching circuit and device itself.

The bias networks have two functions: 1) to isolate the D.C. bias supply to the GaAs FETs from the RF input and output ports of the amplifier circuits; 2) to isolate the biasing system from the RF signals present in the circuit.

D.C. isolation is achieved by inserting an appropriate capacitor into RF circuits, the capacitor value is chosen so that it will self-resonate at the center of frequency band of interest. RF isolation is ensured by feeding the D.C. bias into the circuit via low-pass filter which presents a very high impedance to the circuit at the signal frequencies and also prevents any unpredictable interaction between the RF circuit and the Bias supply and its connecting leads.

In the microwave amplifier, since the low frequency input and output impedances depend strongly on the biasing nework, a development of biasing network having a high insertion loss at low frequencies range is of vital importance.

Figure 4.1.1 shows a bias network, which will be used for the design of 10 Watt solid state power amplifier in Chapter 5.

The circuit uses a microstrip-line quarter-wave transformer with 100 ohm characteristic impedance to simulate an RF choke, another transformer with 20 ohms (low) characteristic impedance in series with RF choke acting as a shunt capacitor at 8GHz, which provides an RF short circuit. The RC circuit (50 ohm chip resistor in series with 82 pF chip capacitor) in parallel with 1000 pF D.C. feed-through circuit is required to increase the insertion loss at low frequencies.

Taking the NE72089, for example, the unstable impedance regions of the input and the output ports of the device are shown in Figure 4.1.1 and Figure4.1.2. It is noted that the device is potentially unstable in the frequency range from 100 MHz to 2000 MHz. By applying the bias network as shown in Figure 4.1.1, a two-stage-NE72089 amplifier is constructed. With the aid of COMPACT^{TM} software, the analysis results are shown in Table 4.1.1.It is interesting to note that the insertion loss is very high from 100 MHz to 2000 MHz and K factor is equal to 999.99, i.e., the amplifier is stable at low frequencies, hence the bias network is doing a good job.

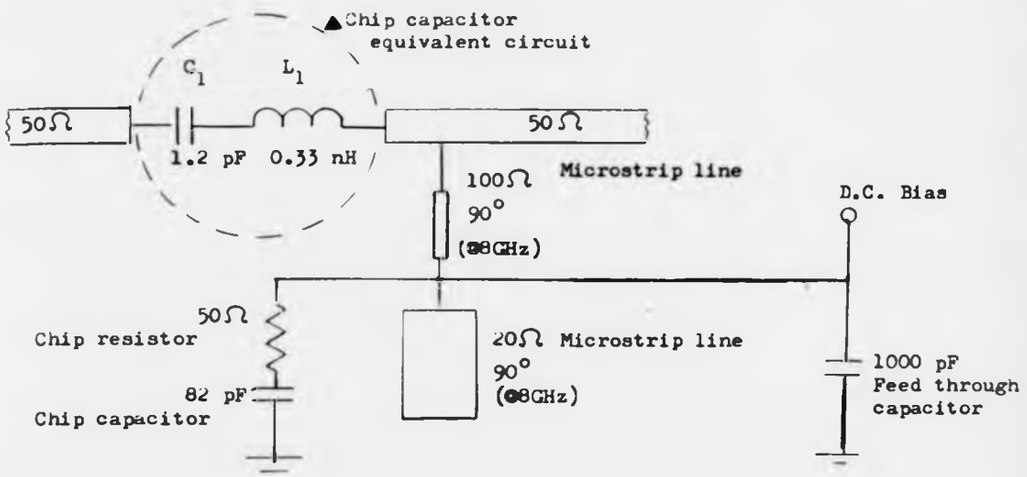


Figure 4.1.1 Bias network for 8 GHz amplifier.

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN	ANGL)	S21 (MAGN	ANGL)	S12 (MAGN	ANGL)	S22 (MAGN	ANGL).	S21 DB	K FACT.
100.00	.36(	127	.00(	-117.4	-50.5DB	-117.4	.35(	127	-50.46	999.99
200.00	.16(	105	.02(	156.2	*****DB	-29.8	.15(	103	-32.93	999.99
500.00	.06(	-103	.05(	22.7	*****DB	-145.3	.07(	-126	-26.10	999.99
1000.00	.24(	-131	.03(	-42.4	*****DB	153.6	.23(	-137	-29.45	999.99
2000.00	.40(	180	.03(	-53.1	*****DB	176.9	.41(	176	-31.44	999.99
4000.00	.68(	-92	2.14(	161.6	-55.1DB	47.6	.62(	-2	6.62	43.22
6000.00	.79(	147	4.41(	173.1	.003(	84.1	.72(	-137	12.88	2.68
7000.00	.55(	110	6.38(	35.0	.017(	-33.0	.36(	150	16.09	2.83
8000.00	.29(	23	7.18(	-98.3	.023(	-146.3	.33(	152	17.12	2.51
9000.00	.24(	177	5.50(	98.4	.023(	70.4	.28(	-58	14.81	3.42
10000.00	.30(	174	3.19(	-60.2	.017(	-72.2	.67(	-100	10.07	2.37
12000.00	.40(	16	.74(	95.8	.006(	103.8	.85(	-153	-2.56	27.32

Table 4.1.1 Analysis results of NE72089 amplifier using the above bias network.

4.2 USING SMITH CHART FOR APPROXIMATE DESIGN AND OPTIMIZATION WITH COMPUTER

4.2.1 General

The impedance matching networks are usually constructed of L sections. See Figure 4.2.1.

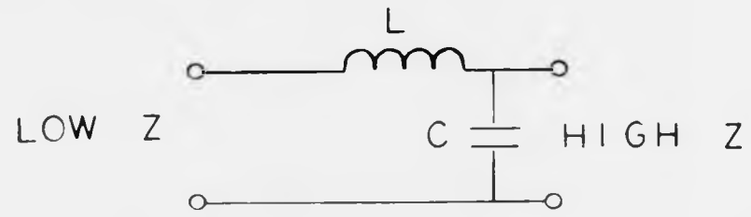


Figure 4.2.1 L Matching Network

In addition to matching these L sections provide a low-pass filter for input and output to keep harmonics down. If the Q of each matching step is kept low, the bandwith of the resulting will be wider. The Q referred to here is the loaded Q of the matching network rather than the unloaded Q of any individual component. In addition to wide bandwidth, low Q matching networks require less critical component values. The values for the L, C and Q may be quickly determined using the Smith chart once the impedance to be matched has been determined.

In designing a matching network, it is convenient to work from the transistor to the 50 ohm termination. If the first matching component is a shunt element the parallel equivalent impedance should be used. Use the series equivalent when the first matching component is a series element.

When working on the Smith chart, always begin with the load that network sees on that end. The final value one obtains at the other end of the network is the impedance one sees looking into the network.

4.2.2 Output Matching Network

The design method for linear amplifier , as a pre-amplifier or a driver of the power amplifier, is probably best illustrated by an example as follows.

Consider the design of a linear amplifier at 8 GHz (bandwidth: 7.725 GHz - 8.275 GHz), using the FLC081WF, its S-parameters are shown in Table 4.2.2.1.

FLC 081WF	(Vds= 10.00 V Ids= 200.00 ma) : S-parameters							
FREQ(Mhz)	S11m	S11a	S21m	S21a	S12m	S12a	S22m	S22a
2000.00	.855	-124.00	3.674	89.00	.054	21.00	.413	-68.00
3000.00	.846	-149.00	2.602	68.00	.054	10.00	.418	-84.00
4000.00	.836	-167.00	2.196	50.00	.054	3.00	.423	-94.00
5000.00	.825	169.00	1.880	29.00	.054	-6.00	.416	-108.00
6000.00	.822	147.00	1.644	10.00	.054	-16.00	.416	-125.00
7000.00	.828	131.00	1.433	-11.00	.054	-25.00	.425	-148.00
8000.00	.819	119.00	1.256	-29.00	.054	-36.00	.439	-165.00
9000.00	.805	107.00	1.091	-50.00	.055	-46.00	.460	176.00
10000.00	.792	97.00	.980	-65.00	.059	-56.00	.488	161.00
11000.00	.783	81.00	.902	-83.00	.066	-63.00	.526	144.00
12000.00	.779	65.00	.853	-100.00	.081	-68.00	.530	129.00

Table 4.2.2.1 S-parameters of the FLC081WF

Using the computer program developed in Chapter 3, the unstable region at the output port is shown in Figure 4.2.2.1, the unstable problem at frequencies below 2GHz can be solely solved by the bias network itself, as described in Section 4.1.

Figure 4.2.2.2 shows the computer results for the FLC081WF at 8 GHz.

FLC 081WF (Vds= 10.00 V Ids= 200.00 ma)

STABILITY CIRCLE

		INPUT PLANE			OUTPUT PLANE		
		Origin		Radius	Origin		Radius
FREQ(Mhz)	K	CSmag	CSang	Rads	CLmag	CLang	Radl
8000.00	1.65	1.18	241.81	.12	1.89	170.24	.65

STABILITY region: UNCONDITION UNCONDITION

Rs1mod/Rs1: 1.182 / .116 ;Rs2mod/Rs2: 1.885 / .646 ; MSG = 13.666 dB

SIMULTANEOUS MATCH FOR MAXIMUM GAIN

FREQ(MHz)	Gmax (dB)	Input match Imp. ZSmag	ZSang	Output match Imp. ZLmag	ZLang
8000.00	8.94	.88	241.81	.65	170.24

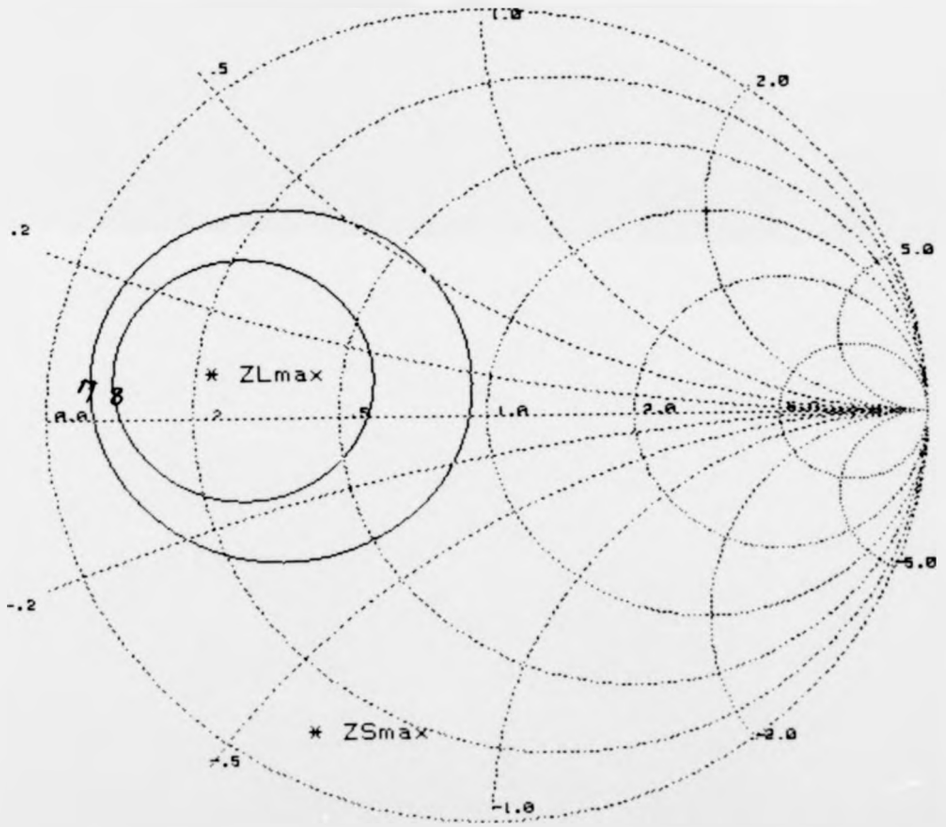


Figure 4.2.2.2 The computer results for the FLC081WF @ 8GHz

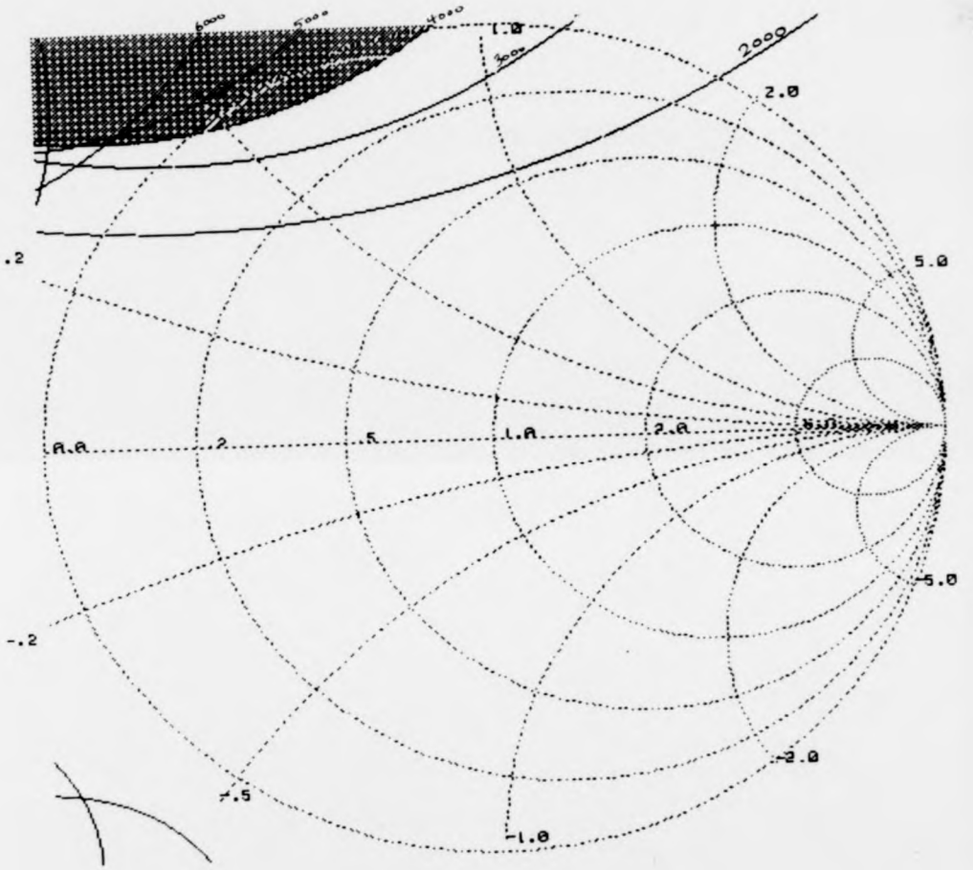


Figure 4.2.2.1 The unstable regions at the output port of the FLC081WF

The output model of the transistor is obtained from the $\rho_{LD} = 0.65 \angle -170^{\circ}$, which is the conjugate of the ZL_{max} in Figure 4.2.2.2.

A circular arc whose center is the center of the Smith chart is drawn through ρ_{LD} and the real axis at point r_L (SEE Figure 4.2.2.3), which is 0.22, corresponding to the pure resistance $R_L = 0.22 \times 50$ ohm = 11 ohm; the distance between ρ_{LD} and r_L is 0.014λ at 8GHz, or the phase angle θ_1 is equal to

$$0.014 \times 360^{\circ} = 5^{\circ}$$

In order to match 11 ohms to 50 ohms, an intermediate impedance Zm is introduced, Zm is given by

$$(11 \times 50)^{1/2} = 23.45 \text{ ohms}$$

The impedance matching networks are constructed of L matching sections as shown in Figure4.2.2.4.

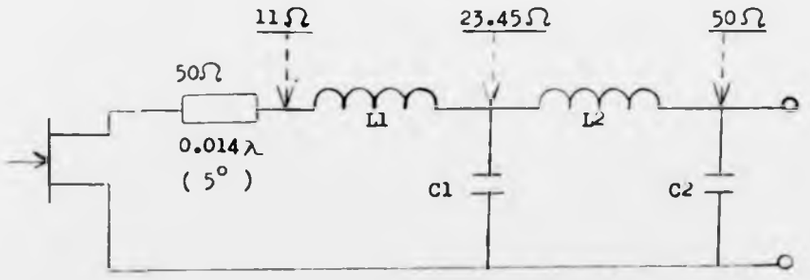


Figure 4.2.2.4 The Output matching network of FLC081WF

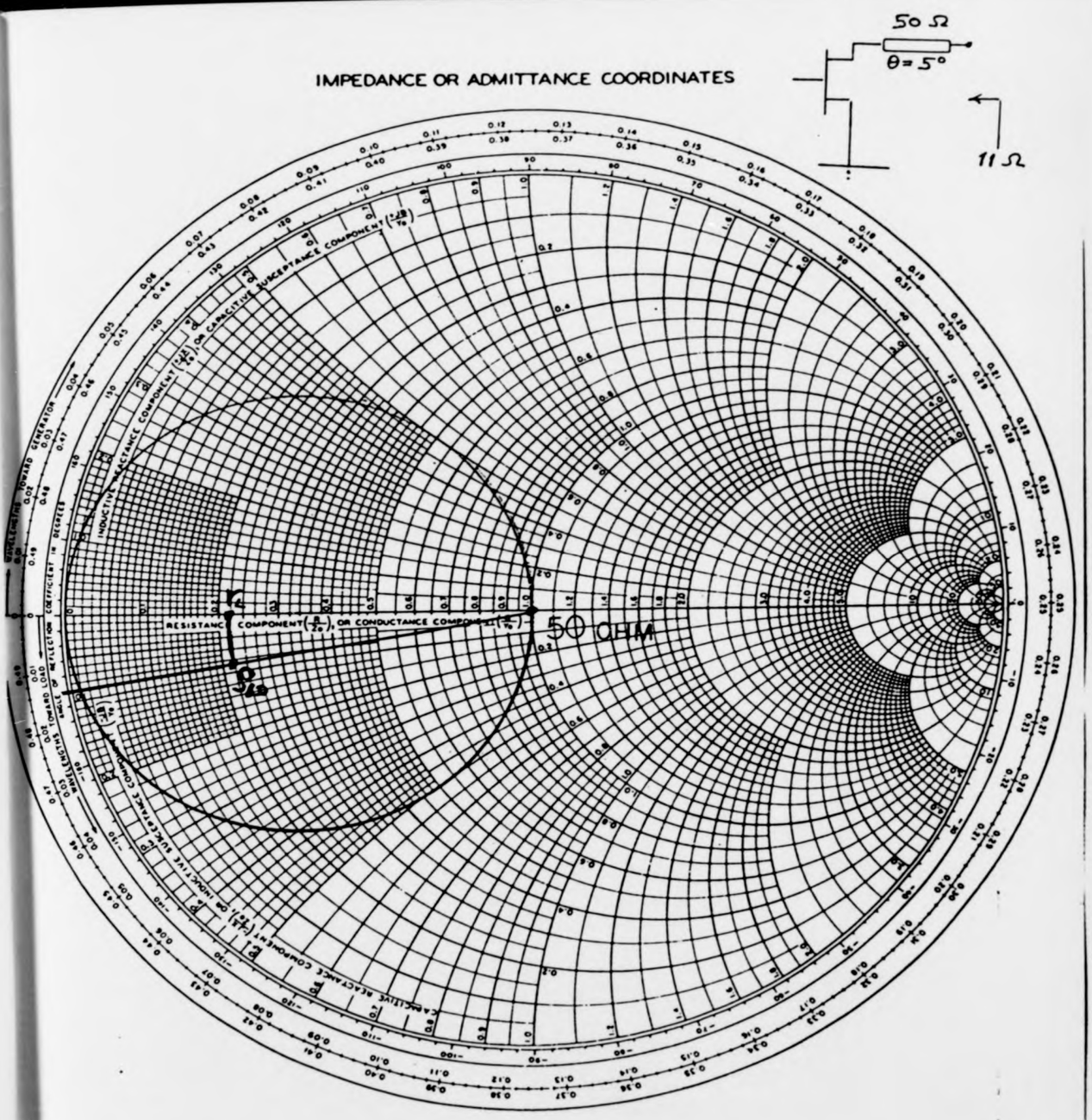


Figure 4.2.2.3. The output model of the FLC081WF is obtaind from tne ρ_{LD}.

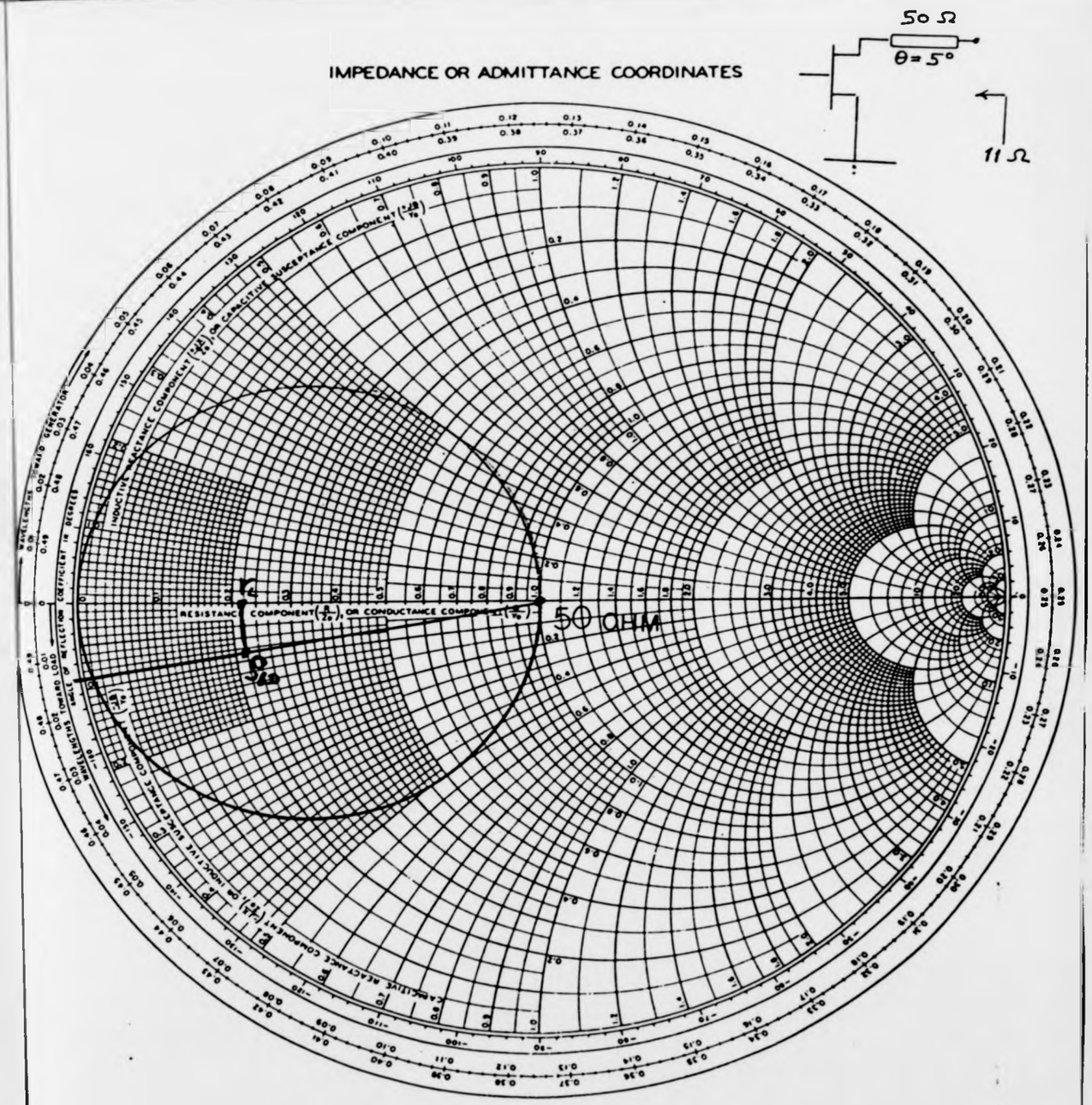


Figure 4.2.2.3. The output model of the FLC081WF is obtaind from tne ρ_{LD}.

Since both the intermediate impedance point and the number of L sections are not critical unless maximum band width is required, Zm is chosen to be 24 ohms (rounded number).

In order to obtain the values of first L section (L1 and C1), the Smith chart as shown in Figure 4.2.2.4 is used, which is normalized to 24 ohms. A calculation begins at 11 ohms (normalized impedance = 0.45 + j 0.0)on the chart and progresses clockwise on a circular path, with the chart center as the origin, until one reaches an admittance circle which also passes through the desired output impedance($Zm = 24\Omega$), the values of L1, C1 and Q can be directly read from the chart, since the final circuit to be realized is microstrip line, instead of a lumped element,L1 can be realized in distributed microstrip line with 24 ohms of characteristic impedance and the length being equal to 0.094λ, λ is the wavelength at 8 GHz. Shunt capacitor C1 can also be considered as 50 ohms characteristic impedance open circuit stub. The length of the parallel open stub is determined as follows:

$$\ominus = \text{arc Cot } (Z_{C1} / Z_o) \qquad (4.2.2.1)$$

$$l_{open} = \ominus / 360^\circ \qquad (4.2.2.2)$$

where $\ominus$ is the phase angle in degree

Z_{C1} is the impedance of the shunt capacitor

Z_o is the characteristic impedance of the open stub.

l_{open}: the normalized wavelength.

Similarly, the Smith chart as shown in Figure 4.2.2.5, which is normalized to 50 ohms, is used to obtain the values of second matching L section. A completed output matching network is shown in Figure 4.2.2.6.

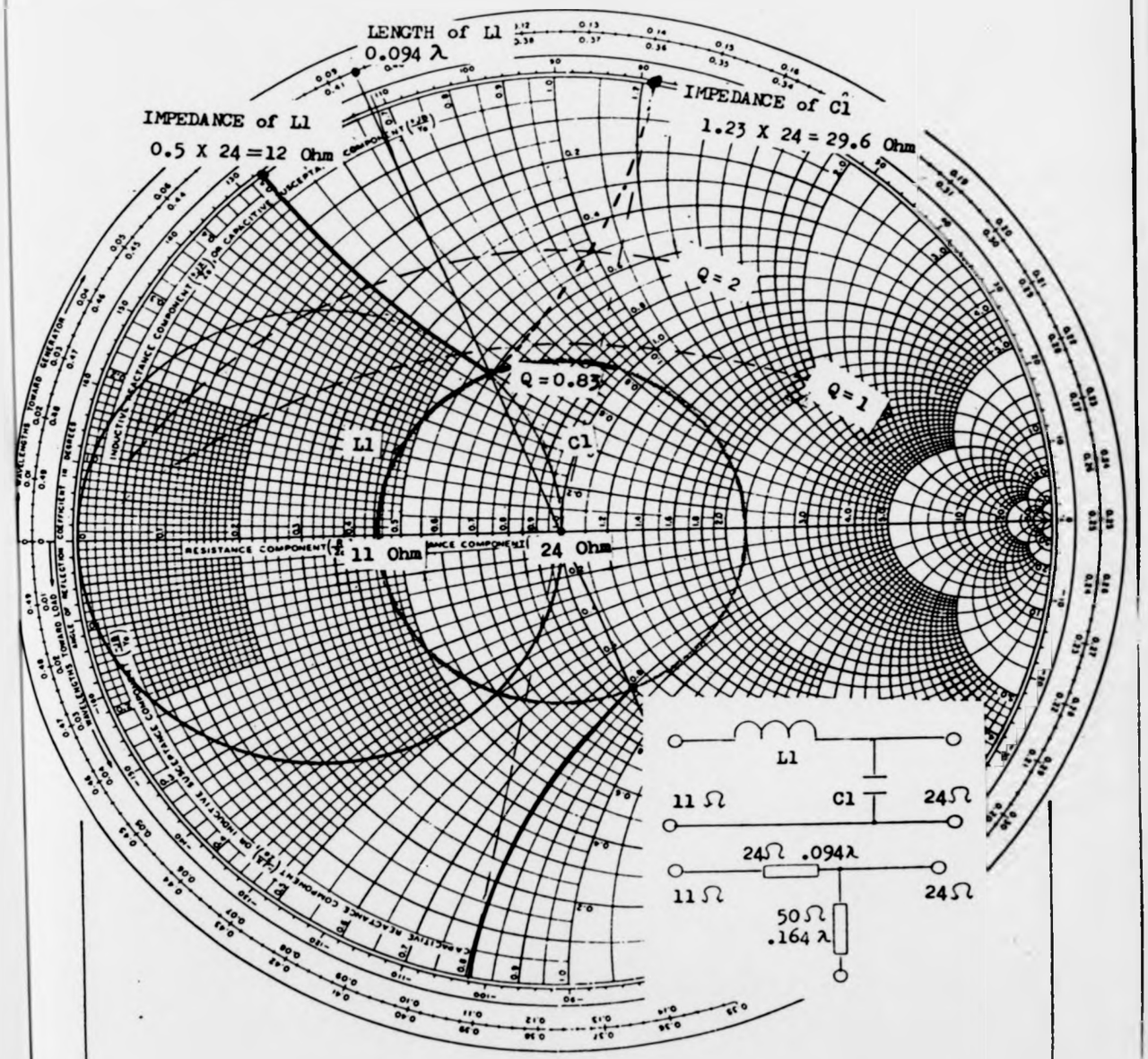


Figure 4.2.2.4 First L Section for Output Matching Network of FLC081WF

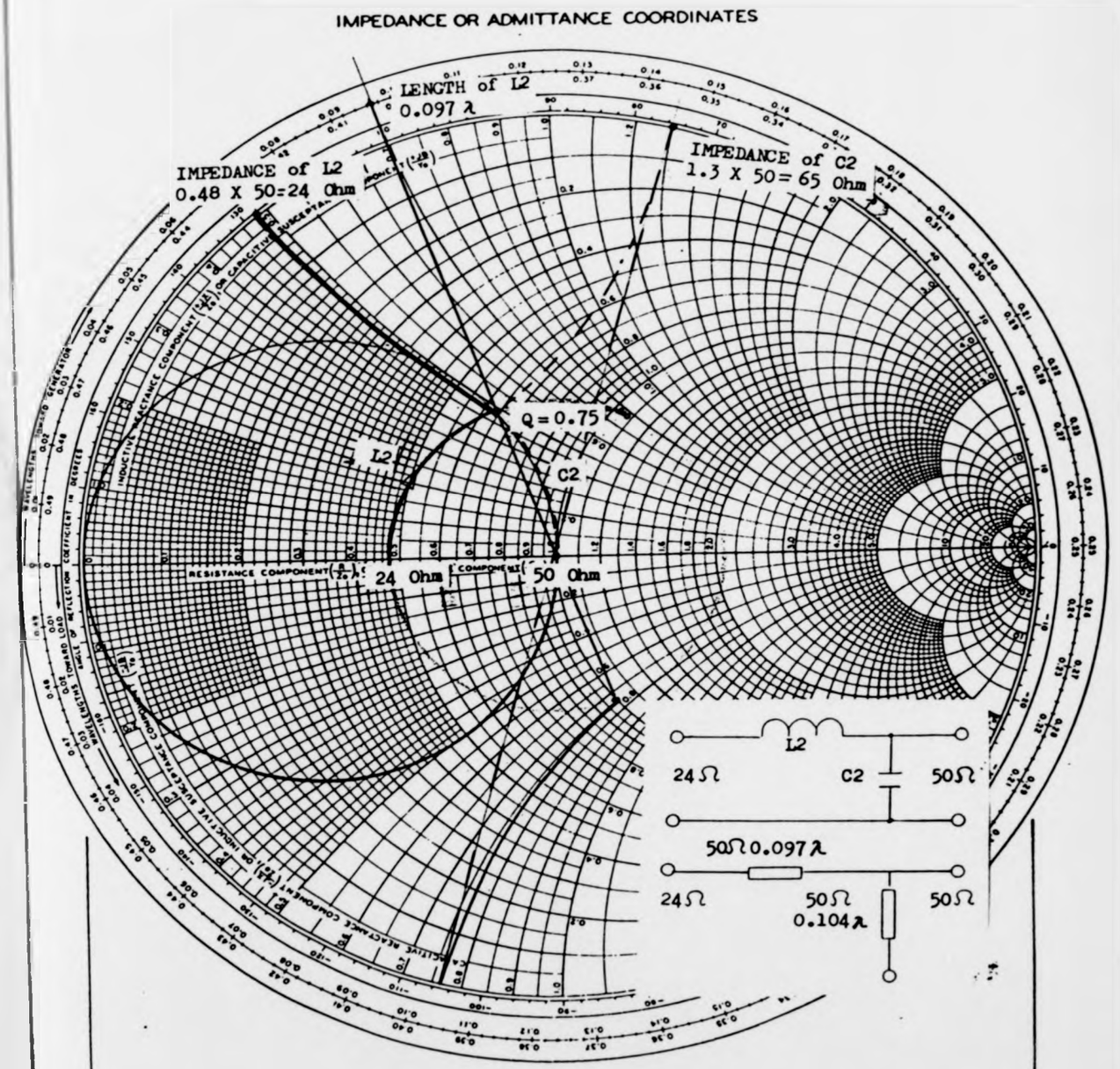


Figure 4.2.2.5 Second L Section for Output Matching Network of FLC081WF

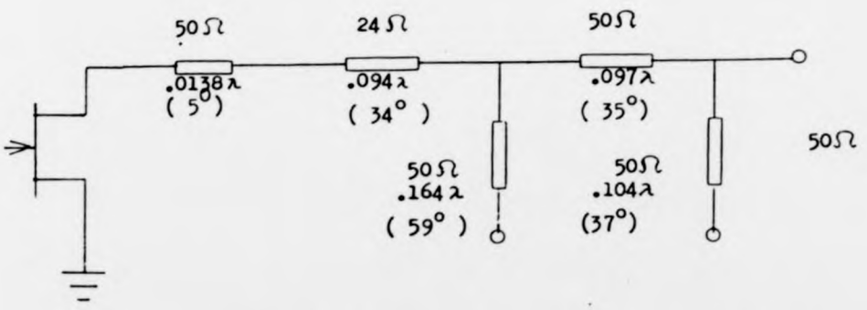


Figure 4.2.2.6 Output Matching Network of FLC081WF.

4.2.3 Input Matching Network

Using the computer program described in Chapter 3, the unstable region at the input port of the FLC081WF is shown in Figure 4.2.3.1. Again, as mentioned in the section 4.1, it will not cause any unstable problem at low frequencies, if the appropriate bias network is applied to the input port of the transistor.

The input model of the transistor is determined as $\rho_{sD} = 0.88 \angle 118^{\circ}$, which is the conjugate of the ZSmax (See Figure 4.2.2.2).

By careful examination of ρ_{sD} , located on the Smith chart as shown in Figure 4.2.3.2, it is found that the input impedance of the transistor at 8 GHz appears to be low resistive and high inductive, therefore the loaded Q is very high (Q= 7.5) .

In order to maintain the lowest loaded Q for the first matching step, the first component used should be a shunt capacitor equal in impedance to that of inductor.

In Figure 4.2.3.2, it is noted that ρ_{sD} is 118° away from real axis, the phase angle Θ can be calculated as

$$\Theta = \frac{118^{\circ}}{180^{\circ}} \times 90^{\circ}$$
$$= 59^{\circ}.$$

Therefore the length of parallel open stub with 50 ohms characteristic impedance is equal to $(59^{\circ}/360^{\circ})\lambda$, 0.164λ.

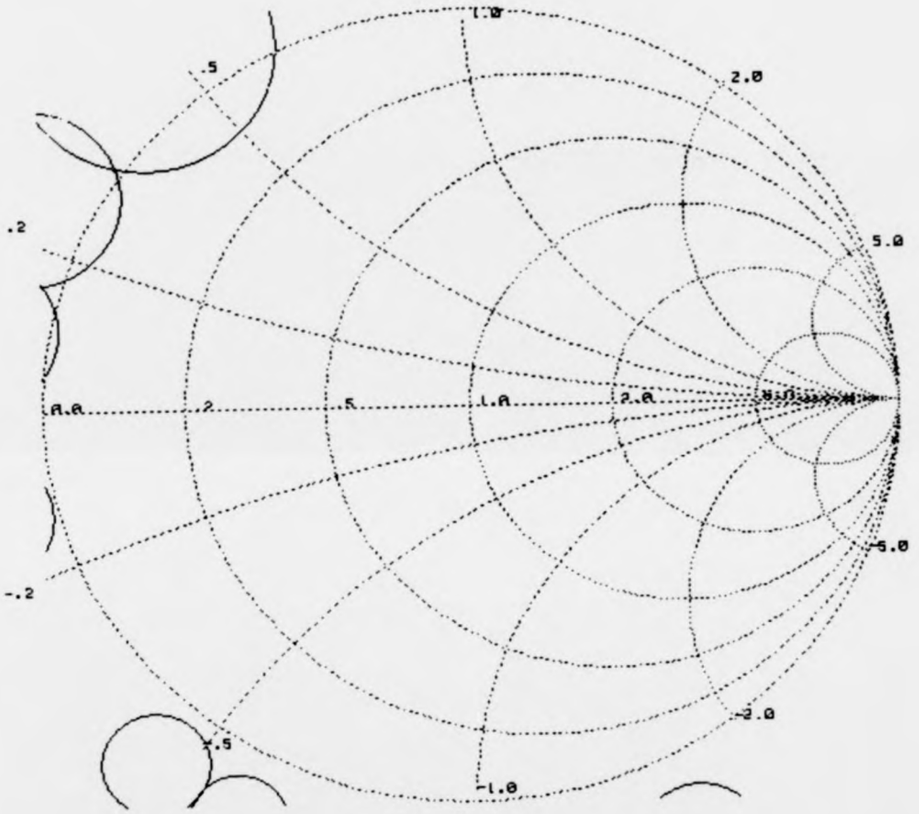


Figure 4.2.3.1 The unstable regions at the Input port of the FLC081WF

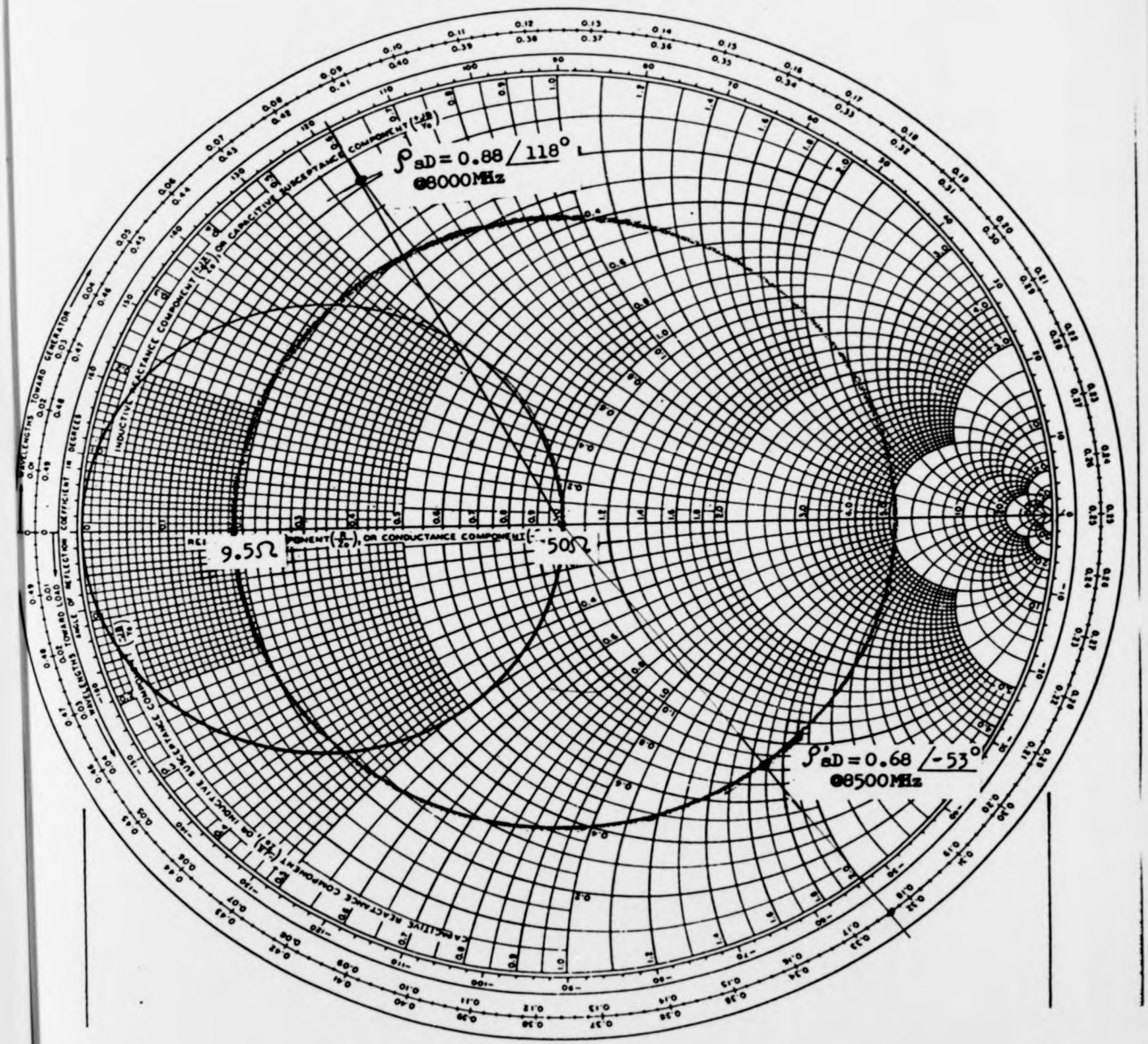


Figure 4.2.3.2 The Input Model of the FLC081WF is obtained from modified ρ_{sD} to ρ'_{sD}.

With a shunt element added on the input port of the FLC081WF as shown in Figure 4.2.3.3, a new set of S-parameters is shown in Table 4.2.3.2; the analysis is done by COMPACT™ , the COMPACT data file for creating a S-parameters is in Table 4.2.3.1.

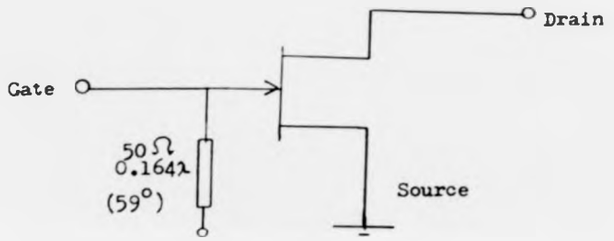


Figure 4.2.3.3 Modified the input port of the FLC081WF for lowing the loaded Q.

```
COMPACT VERSION 5.1 COMMAND FILE

COMMAND FILE==> FLC081
OST AA PA 50 59 8000
TWO BB S1 50
CAX AA BB
PRI AA S4 50
END
7000 9000 500
END
.83 131 1.43 -11. .054 -25 .43 -148
.83 125 1.34 -19.9 .054 -30.4 .43 -157
.82 119 1.26 -29 .054 -36 .44 -165
.81 113 1.17 -39.8 .054 -41.1 .45 -175
.81 107 1.09 -50 .055 -46 .46 176
END
```

Table 4.2.3.1 COMPACT data file for creating a new set of S-parameters for modified FLC081WF

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN<ANGL)	S21 (MAGN<ANGL)	S12 (MAGN<ANGL)	S22 (MAGN<ANGL)	S21 DB	K FACT.
7000.00	.55< 88	2.14< -36.4	.081< -50.4	.50< -148	6.59	1.34
7500.00	.48< 50	2.11< -56.5	.085< -67.0	.51< -160	6.50	1.45
8000.00	.46< -4	1.96< -80.2	.084< -87.2	.51< -172	5.84	1.63
8500.00	.58< -56	1.63<-107.0	.075<-108.3	.49< 176	4.24	1.86
9000.00	.75< -91	1.24<-132.5	.063<-128.5	.47< 167	1.86	1.94

POLAR COORDINATES OF SIMULTANEOUS CONJUGATE MATCH

F MHZ	SOURCE REFL. COEFF. MAGN.<ANGLE	LOAD REFL. COEFF. MAGN.<ANGLE	GMAX DB
7000.0	.73< -84	.71< 154	10.73
7500.0	.66< -48	.68< 163	9.97
8000.0	.62< 2	.65< 170	9.02
8500.0	.68< 53	.63< 180	8.01
9000.0	.81< 90	.63<-172	7.41

Table 4.2.3.2 S-parameters for modified FLC081WF

Since the gain of the transistor is rolling off with increasing frequency, it is desirable to model the input of the transistor based on the information from higher edge of the frequency band. Therefore, the input model of the transistor is obtained from $\rho'_{sD} = 0.68 \angle -53^{\circ}$, which is the conjugate of the source reflection coeffecient at 8.5GHz under simultaneous matched condition.

A circular arc whose center is the center of the Smith chart is drawn tnrough ρ_{sD}' and the real axis at 0.19 of normalized resistance ; tne corresponding impedance is equal to 9.5 ohms, the electrical length is 0.176λ, see Figure 4.2.3.2.

The method for matching tne impedance between 9.5 ohms and 50 ohms has been described in Section 4.2, with the aid of the Smitn charts as snown in Figures 4.2.3.4 and 4.2.3.5 and the input matcning network is obtained in Figure 4.2.3.6.

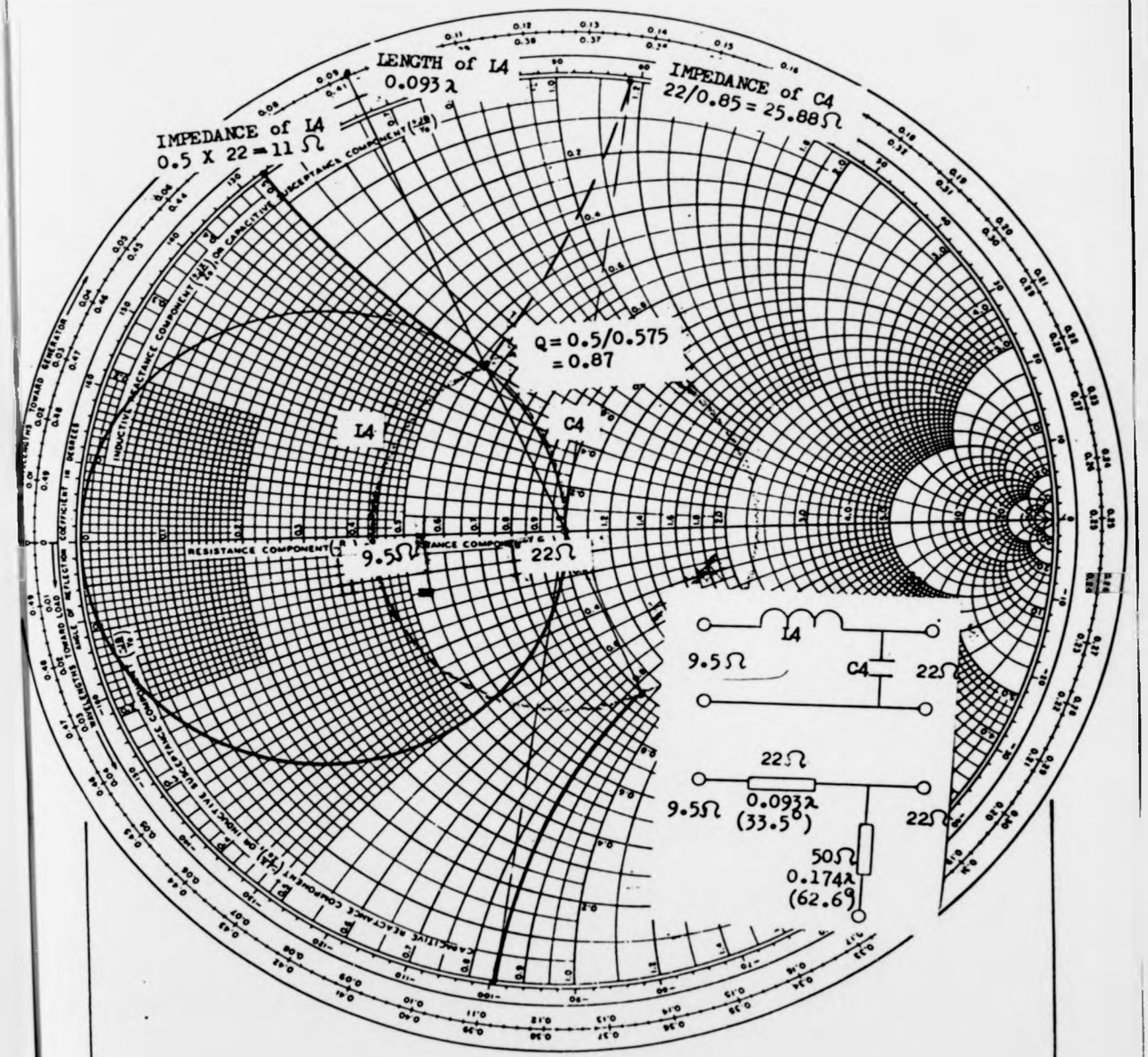


Figure 4.2.3.4 First L Section for Input Matching Network of FLC081WF

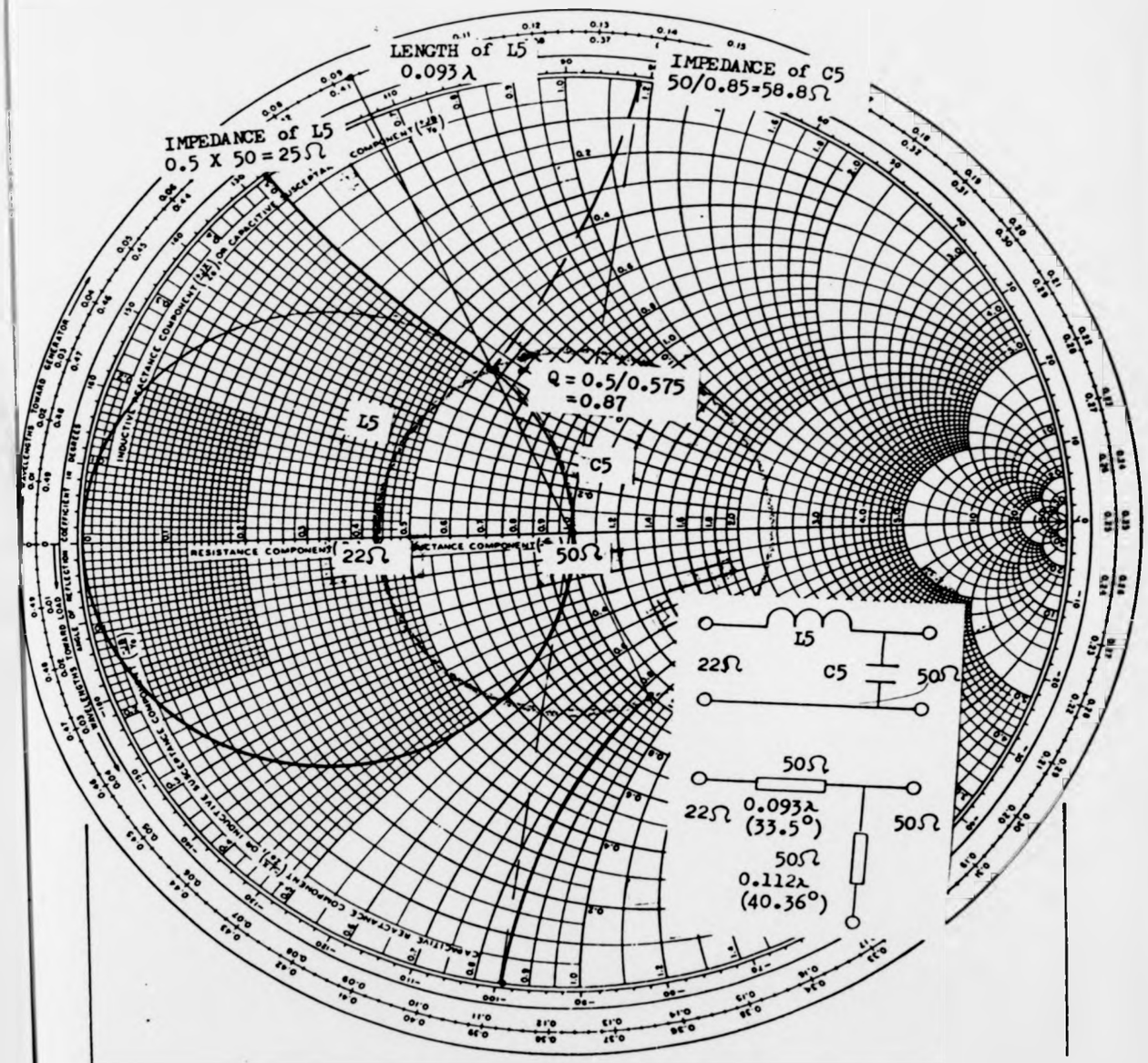


Figure 4.2.3.5 Second L Section for Input Matching Network of FLC081WF

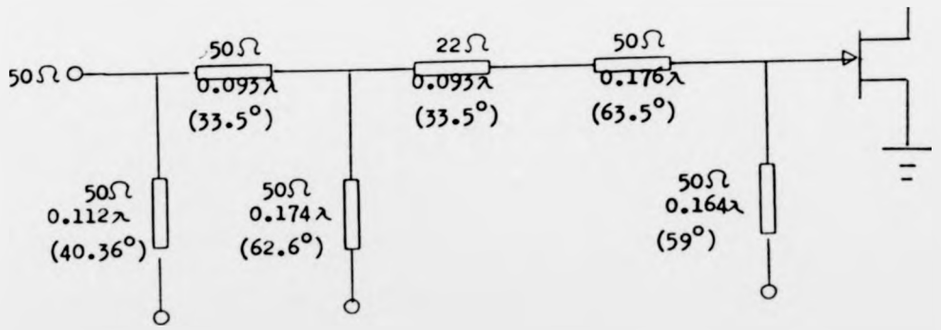


Figure 4.2.3.6 Input Matching Network of FLC081WF

Table 4.2.3.3 is the COMPACT data file for analysis of the FLC081WF amplifier, the initial circuit analysis results are in Table 4.2.3.3. It is interesting to note that at 8.5GHz , the gain is 7.76 dB, while the theoretical maximum gain with simultaneous match of both the input and output ports is 8.01 dB; the difference is only 0.25 dB.

```
OST AA PA 50 -40.36 8500
TRL BB SE 50 -33.5 8500
OST CC PA 50 -62.6 8500
TRL DD SE 22 -33.5 8500
TRL EE SE 50 -63.5 8500
OST FF PA 50 -59 8000
TWO GG S1 50
TRL HH SE 50 -5 8000
TRL II SE 24 -34 8000
OST JJ PA 50 -59 8000
TRL KK SE 50 -35 8000
OST LL PA 50 -37 8000
CAX AA LL
PRI AA S4 50
END
7000 7500
8000
8500 9000
END
```

Table 4.2.3.3 The COMPACT file for analysis the FLC081WF amplifier with input and output matching networks design from this Chapter.

INITIAL CIRCUIT ANALYSIS

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN<ANGL)	S21 (MAGN<ANGL)	S12 (MAGN<ANGL)	S22 (MAGN<ANGL)	S21 DB	K FACT.
7000.00	.93< 166	1.15< 92.2	.043< 78.2	.47< 129	1.21	1.34
7500.00	.90< 147	1.35< 62.9	.054< 52.4	.39< 117	2.60	1.45
8000.00	.75< 116	1.88< 22.0	.081< 15.0	.24< 98	5.48	1.63
8500.00	.07< -120	2.44< -59.5	.113< -60.8	.24< -169	7.76	1.86
9000.00	.83< 161	1.19<-143.6	.060<-139.6	.51< 141	1.51	1.94

Table 4.2.3.4. The analysis results from the COMPACT

Table 4.2.3.3 is the COMPACT data file for analysis of the FLC081WF amplifier, the initial circuit analysis results are in Table 4.2.3.3. It is interesting to note that at 8.5GHz , the gain is 7.76 dB, while the theoretical maximum gain with simultaneous match of both the input and output ports is 8.01 dB; the difference is only 0.25 dB.

```
OST AA PA 50 -40.36 8500
TRL BB SE 50 -33.5 8500
OST CC PA 50 -62.6 8500
TRL DD SE 22 -33.5 8500
TRL EE SE 50 -63.5 8500
OST FF PA 50 -59 8000
TWO GG S1 50
TRL HH SE 50 -5 8000
TRL II SE 24 -34 8000
OST JJ PA 50 -59 8000
TRL KK SE 50 -35 8000
OST LL PA 50 -37 8000
CAX AA LL
PRI AA S4 50
END
7000 7500
8000
8500 9000
END
```

Table 4.2.3.3 The COMPACT file for analysis the FLC081WF amplifier with input and output matching networks design from this Chapter.

INITIAL CIRCUIT ANALYSIS

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN<ANGL)	S21 (MAGN<ANGL)	S12 (MAGN<ANGL)	S22 (MAGN<ANGL)	S21 DB	K FACT.
7000.00	.93< 166	1.15< 92.2	.043< 78.2	.47< 129	1.21	1.34
7500.00	.90< 147	1.35< 62.9	.054< 52.4	.39< 117	2.60	1.45
8000.00	.75< 116	1.88< 22.0	.081< 15.0	.24< 98	5.48	1.63
8500.00	.07< -120	2.44< -59.5	.113< -60.8	.24< -169	7.76	1.86
9000.00	.83< 161	1.19<-143.6	.060<-139.6	.51< 141	1.51	1.94

Table 4.2.3.4. The analysis results from the COMPACT

```
COMPACT VERSION 5.1 COMMAND FILE


OST AA PA 50 -51.6894 8500
TRL BB SE 50 -62.6852 8500
OST CC PA 50 -27.9839 8500
TRL DD SE 22 -27.7797 8500
TRL EE SE 50 -126.401 8500
OST FF PA 50 -51.1471 8000
TWO GG S1 50
TRL HH SE 50 -5.63591 8000
TRL II SE 24 -45.3814 8000
OST JJ PA 50 -53.2771 8000
TRL KK SE 50 -46.1935 8000
OST LL PA 50 -46.6156 8000
CAX AA LL
PRI AA S4 50
END
7000
7500
8000
8500 9000
END
.83 131 1.43 -11. .054 -25 .43 -148
.83 125 1.34 -19.9 .054 -30.4 .43 -157
.82 119 1.26 -29 .054 -36 .44 -165
.81 113 1.17 -39.8 .054 -41.1 .45 -175
.81 107 1.09 -50 .055 -46 .46 176
END
0.01
10 10 1 7
10 10 1 6
10 10 1 7
10 10 1 8
END
```

Table 4.2.3.5 COMPACT data file after optimization for The FLC081WF amplifier.

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN< ANGL)	S21 (MAGN< ANGL)	S12 (MAGN< ANGL)	S22 (MAGN< ANGL)	S21 DB	K FACT.
7000.00	.71< 53	2.24< 3.9	.085< -10.1	.25< 40	7.01	1.34
7500.00	.63< -21	2.29< -50.2	.092< -60.7	.15< -22	7.21	1.45
8000.00	.59< -88	2.15< -102.5	.092< -109.5	.15< -79	6.64	1.63
8500.00	.47< -152	2.14< -159.3	.099< -160.6	.15< -128	6.62	1.86
9000.00	.40< 56	2.12< 122.8	.107< 126.8	.11< 106	6.53	1.94

Table 4.2.3.5 The final results after optimization

Table 4.2.3.5 shows the final results of the FLC081WF amplifier at 8 GHz with 25% bandwidth (i.e. 2000 MHz), the gain is 6.87 dB $\pm$ 0.34 dB; for 12.5% bandwidth (i.e. 1000 MHz) the gain is 6.915 dB $\pm$ 0.295 dB.

4.3 Third-order Intermodulation Theory (2)

One of the most common nonlinearity characterization of a two-port network is its amplitude distortion, which results in its nonlinear transfer characteristic. If the two-port network is memoryless, that is, its output voltage is an instantaneous function of its input voltage, and its nonlinearity weak which is the case of most communication system then the output voltage $e_o(t)$ can be represented by a power series of the input voltage $e_i(t)$ as

$$e_o(t) = k_1 e_i(t) + k_2 e_i(t)^2 + k_3 e_i(t)^3 \tag{4.3.1}$$

Consider an input signal

$$e_i(t) = A(\cos\omega_1 t + \cos\omega_2 t) \tag{4.3.2}$$

that consists of two equal amplitude sinusoids at two different frequencies ω_1 and ω_2.

Applying e_i to Eqn.(4.3.1) yields

$$\begin{aligned} e_o(t) &= k_1 A(\cos\omega_1 t + \cos\omega_2 t) + k_2 A^2(\cos\omega_1 t + \cos\omega_2 t)^2 + k_3 A^3(\cos\omega_1 t + \cos\omega_2 t)^3 \\ &= k_2 A^2 + k_2 A^2 \cos(\omega_1 - \omega_2)t + (k_1 A + \tfrac{9}{4} k_3 A^3)\cos\omega_1 t \\ &\quad + (k_1 A + \tfrac{9}{4} k_3 A^3)\cos\omega_2 t + \tfrac{3}{4} k_3 A^3 \cos(2\omega_1 - \omega_2)t \\ &\quad + \tfrac{3}{4} k_3 A^3 \cos(2\omega_2 - \omega_1)t + k_2 A^2 \cos(\omega_1 + \omega_2)t + \tfrac{1}{2} k_2 A^2 \cos 2\omega_1 t \\ &\quad + \tfrac{1}{2} k_2 A^2 \cos 2\omega_2 t + \tfrac{3}{4} k_3 A^3 \cos(2\omega_1 + \omega_2)t + \tfrac{3}{4} k_3 A^3 \cos(2\omega_2 + \omega_1)t \\ &\quad + \tfrac{1}{4} k_3 A^3 \cos 3\omega_1 t + \tfrac{1}{4} k_3 A^3 \cos 3\omega_2 t \end{aligned} \tag{4.3.3}$$

From Eqn.(4.3.3) it is seen that the output signal consists of components at dc, the fundamental frequencies ω_1 and ω_2, the second and third harmonics $2\omega_1, 2\omega_2$, and $3\omega_1$, $3\omega_2$ and the second-order intermodulation products at $\omega_1 \pm \omega_2$ (the sum of the coefficients of ω_1 and ω_2 is 2), and the third-order intermodulation products at $2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ (the sum of the coefficients of ω_1 and ω_2 is 3). In the system where the operating frequency band is less than an octave, all the spurious signals at $\omega_1 \pm \omega_2$, $2\omega_1$, $2\omega_2$, $2\omega_1 + \omega_2$, $2\omega_2 + \omega_1$, $3\omega_1$ and $3\omega_2$ fall outside the passband and can be attenuated by appropriate filters. But all the spurious signals at the frequencies $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ will fall within the passband and can distort the desired signal at the fundamental frequency ω_1 or ω_2. The input and output spectrum of e_i and e_o are shown in Figure 4.3.1 (a)-(b).

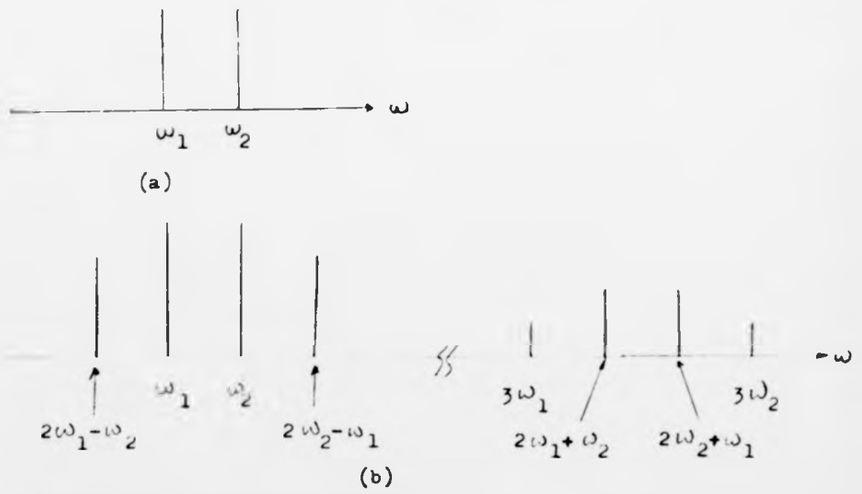


Figure 4.3.1 (a) Input Spectrum
(b) Output Spectrum of a two-port with third-order Distortion

Consider an input signal with single frequency ω_1

$$e_i = A\cos\omega_1 t \tag{4.3.4}$$

Applying Eqn.(4.3.4) to Eqn.(4.3.1) yields

$$\begin{aligned} e_o(t) &= k_1 A\cos\omega_1 t + k_2 A^2\cos^2\omega_1 t + k_3 A^3\cos^3\omega_1 t \\ &= k_1 A\cos\omega_1 t + k_2 A^2\left(\tfrac{1}{2} + \tfrac{1}{2}\cos 2\omega_1 t\right) + k_3 A^3\left(\tfrac{3}{4}\cos\omega_1 t + \tfrac{1}{4}\cos 3\omega_1 t\right) \\ &= \tfrac{1}{2}k_2 A^2 + \left(k_1 A + \tfrac{3}{4}k_3 A^3\right)\cos\omega_1 t + \tfrac{1}{2}k_2 A^2\cos 2\omega_1 t + \tfrac{1}{4}k_3 A^3\cos 3\omega_1 t \end{aligned} \tag{4.3.5}$$

From Eqn.(4.3.5), one can see that the fundamental component of e_o has an amplitude of $k_1 A\left[1 + \frac{3}{4}(k_3/k_1)A^2\right]$, which is greater than $k_1 A$ (the gain if the two-port is linear) if $k_3 > 0$ and smaller than $k_1 A$ if $k_3 < 0$. This property is called gain expansion or gain compression. Most practical devices are compressive, that is, $k_3 < 0$ and the output power is usually characterized at the 1 dB gain compression point.

From Eqn.(4.3.5), the gain at the fundamental frequency ω_1 is given by

$$G = 20\log\frac{k_1 A + \frac{3}{4}k_3 A^3}{A} = 20\log\left(k_1 + \tfrac{3}{4}k_3 A^2\right) \tag{4.3.6}$$

as compared to the linear gain G_o defined as

$$G_o = 20\log\frac{k_1 A}{A} = 20\log k_1 \tag{4.3.7}$$

The 1 dB gain compression point is defined as the signal level where

$$G_{1dB} = G_o - 1 \quad \text{dB} \tag{4.3.8}$$

or equivalently,

$$k_1 + \tfrac{3}{4}k_3 A^2 = 0.891\, k_1 \tag{4.3.8a}$$

Hence at the 1 dB gain compression point the amplitude of e_i is limited as

$$A = \left(0.145 \frac{k_1}{|k_3|}\right)^{\frac{1}{2}}, \quad k_3 < 0 \qquad (4.3.8b)$$

Assume that the input and output impedences of the two-port are

$$Z_{in} = Z_{out} = R \qquad (4.3.9)$$

Then the input and output powers P_i and P_o at the fundamental frequency ω_1 are given in dBm as

$$P_i = 10\log\left[\left(\frac{A}{\sqrt{2}}\right)^2 \frac{10^3}{R}\right] \text{ dBm} \qquad (4.3.10)$$

$$P_o = 10\log\left[\left(\frac{k_1 A + \frac{3}{4}k_3 A^3}{\sqrt{2}}\right)^2 \frac{10^3}{R}\right] \text{ dBm}$$

$$= G + P_i \text{ dBm} \qquad (4.3.11)$$

The output power at 1 dB gain compression point P_{1dB} is

$$P_{1dB} = G_{1dB} + P_i = G_o - 1 + P_i \text{ dBm} \qquad (4.3.12)$$

Substituting Eqn.(4.3.8b) and Eqn.(4.3.10) into Eqn.(4.3.12) yields

$$P_{1dB} = G_o - 1 + 10\log\left[\frac{0.145k_1}{2|k_3|} \cdot \frac{10^3}{R}\right] \text{ dBm}$$

$$= 10\log\frac{57.70\, k_1^3}{|k_3| R}$$

$$= 10\log\left(\frac{1}{17.33}\frac{k_1^3}{|k_3|}\frac{10^3}{R}\right) \text{ dBm} \qquad (4.3.13)$$

For $R = 50\Omega$, then

$$P_{1dB} = 10\log\frac{k_1^3}{|k_3|} + 0.62 \text{ dBm} \qquad (4.3.14)$$

A useful measure of the third-order intermodulation distortion is the " intercept point," defined as the output power level P_I at which the output power $P_{(2\omega_1 - \omega_2)}$ at the frequency $2\omega_1 - \omega_2$ would intercept the output power P_o at ω_1 (where the two-port is linear) if low-level results were extrapolated into the higher-power region as shown in Figure 4.3.2. At low level, the ouput power P_o is directly proportional to the amplitude of the input signal while the output power $P_{(2\omega_1-\omega_2)}$ is directly proportional to the cube of the input amplitude.Thus the plot of each on a log-log scale(or dBm/dBm scale) will be a straight line with a slope corresponding to the order of the response, that is, the response at ω_1 will have a slope of 1 and the response at $2\omega_1 - \omega_2$ will have a slope of 3. Their intersection is the intercept point. The actual amplitude of the output signal at ω_1 is $k_1A+\frac{9}{4}k_3A^3$ where $k_3 < 0$ for compressive two-ports. Hence at lower power levels $(k_1A+\frac{9}{4}k_3A^3)$, the response of the output power $P_{(\omega_1)}$ at ω_1 almost coincides with the response of the output power P_o at ω_1 when the two-port is assumed to be linear. At higher power levels the response of $P_{(\omega_1)}$ will be compressed and will deviate from the response of P_o as shown in Figure 4.3.2.

From Eqn.(4.3.3):

$$P_o = 10\log\left[\left(\frac{k_1A}{\sqrt{2}}\right)^2\frac{10^3}{R}\right] \text{ dBm} \qquad (4.3.15)$$

$$P_{(\omega_1)} = 10\log\left[\left(\frac{k_1A + \frac{9}{4}k_3A^3}{\sqrt{2}}\right)^2\frac{10^3}{R}\right] \text{ dBm} \qquad (4.3.16)$$

$$P_{(2\omega_1-\omega_2)} = 10\log\left[\left(\frac{\frac{3}{4}k_3A^3}{\sqrt{2}}\right)^2\frac{10^3}{R}\right] \text{ dBm} \qquad (4.3.17)$$

Since at P_I by definition, $P_o = P_{(2\omega_1 - \omega_2)}$, by comparing Eqns.(4.3.17) and (4.3.15), one obtains the theoretical amplitude A at P_I as

$$A \quad (\text{at } P_I) = \left(\frac{4}{3}\,\frac{k_1}{|k_3|}\right)^{\frac{1}{2}} \qquad (4.3.18)$$

and therefore

$$P_I = 10\log\left(\frac{2}{3}\,\frac{k_1^3}{|k_3|}\,\frac{10^3}{R}\right) \text{ dBm} \qquad (4.3.19)$$

If $R = 50\,\Omega$

$$P_I = 10\log\frac{k_1^3}{|k_3|} + 11.25 \text{ dBm} \qquad (4.3.20)$$

And from Figure 4.3.2, the response of $P_{(\omega_1)}$ intersects the response of $P_{(2\omega_1 - \omega_2)}$ at the point P_I'. It is useful to relate P_I' to P_I. At P_I', $P_{(\omega_1)} = P_{(2\omega_1 - \omega_2)}$. By comparing Eqns.(4.3.16) and (4.3.17) tne amplitude A at P_I' is given as

$$A \quad (\text{at } P_I') = \left(\frac{2}{3}\,\frac{k_1}{|k_3|}\right)^{1/2} \qquad (4.3.21)$$

and hence

$$P_I' = 10\log\left(\frac{1}{1\,2}\,\frac{k_1^3}{|k_3|}\,\frac{10^3}{R}\right) \text{ dBm}$$

$$= P_I - 9 \text{ dBm} \qquad (4.3.22)$$

By comparing Eqns. (4.3.13) and (4.3.19), a relationship between P_I and P_{1dB} is given as

$$P_I = P_{1dB} + 10.63 \text{ dBm} \qquad (4.3.23)$$

From Eqn. (4.3.19), the intercept power P_I is independent of the input power and is therefore a useful measure of the system nonlinearity. Also by comparing Eqns. (4.3.15), (4.3.17) and (4.3.19), the output power at $2\omega_1 - \omega_2$ can be given as

$$P_{(2\omega_1 - \omega_2)} = 3P_o - 2P_I \qquad (3.4.24)$$

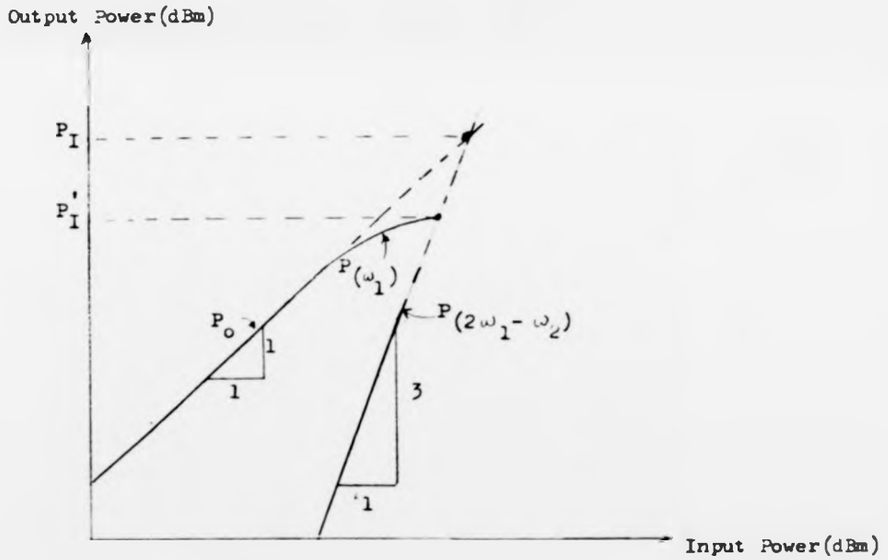


Figure 4.3.2 Definition of the intercept point

Finally, the third order intermodulation distortion IMD_3 in dBc is defined as

$$IMD_3 \ (\text{dBc}) = P_{(2\omega_1 - \omega_2)} - P_{(\omega_1)} \qquad (4.3.25)$$

4.4 Transistor Large Signal Characterization

It is well known that the higher the power of GaAs FETs the wider the total gate width must be. Therefore, the evaluation of high power GaAs FETs become more difficult, because the input impedance of the device become lower, (e.g. for gate width of 1800 um the impedance is only 4 ohms) (3). This will degrade conventional small signal S-parameters measurement.

As the FET is non-linear at high power operation, the small signal S-parameters become inadequate, because the optimum load impedance varies unpredictably with the output power.

Large-signal behaviour is usually described by experimental load-pull data which shows the load dependence of the transistor output power at a fixed input (4)-(8).

The so-called "load-pull" measurement, using ultraprecision calibrated impedance tuner, measures device power output P_{out} by selecting an output load whose impedance Z_L has the opposite sign to impedance Z_{out}, looking into the device output. These measurements produce a series of constant power-output contours on a Smith chart (which show all possible load impedances). To obtain the contours, a measurement must be made at each power level and at each frequency of interest.

A test setup that can be used to measure large-signal load-pull data and third order intermodulation distortion IMD_3 is suggested in Figure 4.4.1. The transistor is first mounted in a suitable test fixture designed so that the reference planes at the input and output of the packaged device can be accurately measured.

Two signal generators are used for measuring third order intermodulation distortion, two single frequencies f_1 and f_2 with 5-10 MHz apart are set to be of equal amplitude. For load-pull measurements , the signal generator f_1 only is used.

The first step in the experimental method is to determine at which input power level the large signal load pull data should be measured. This level is found as follows.(9)

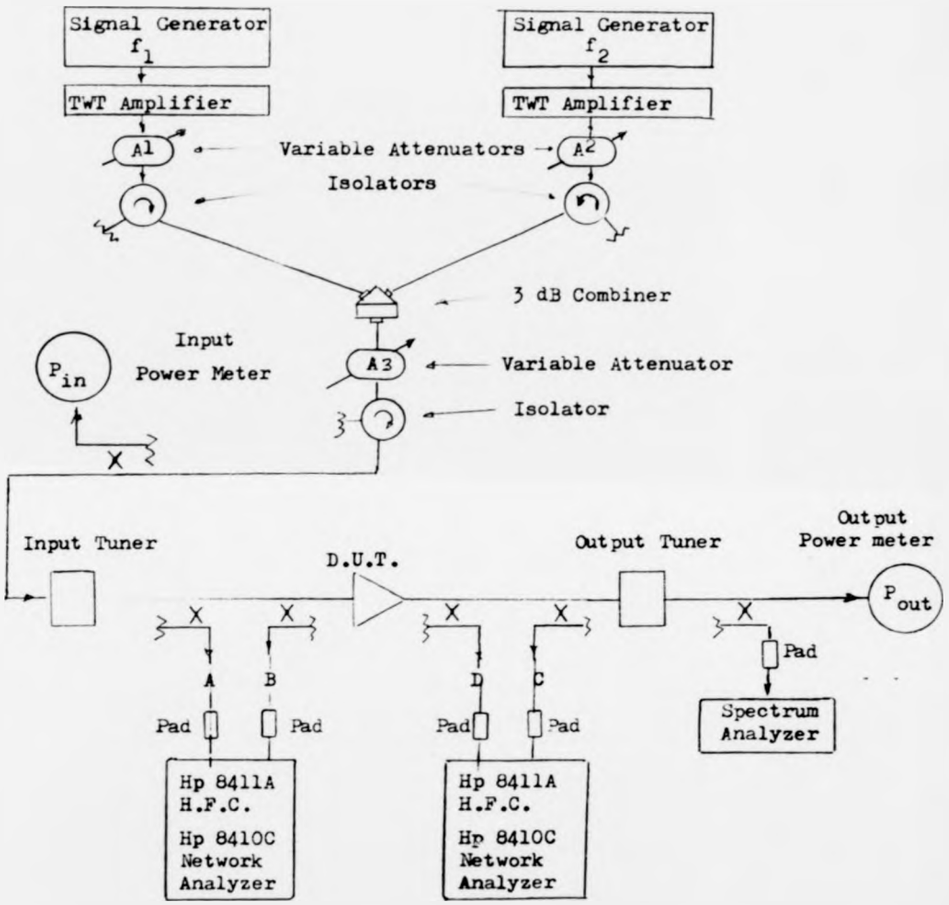


Figure 4.4.1 Test Setup for Measurement of Large Signal Parameter (Load-Pull) and 3rd-order Intermodulation Distortion.

For the MSC 88010 high power device, f_1 is set to be 6.6 GHz , at a number of input power ranging from 20 dBm to 29 dBm (this range may vary depending upon the device under test). The input tuner and output tuner are set to yeild the maximum gain, then with the tuners remaining fixed, the small signal gain is measured and the compression is calculated, until 1 dB gain compression point is found, which is 28 dBm for the MSC88010.

The second step is to adjust the input and output tuners for maximum output power gain with 28 dBm input power level. Then keeping the input tuner fixed, the output tuner is varied to obtain constant power gain. By setting f_2 equal to 6.605 GHz, the third order intermodulation distortion IMD_3 is also measured. Next, the gain, load impedance and IMD_3 are recorded for a number of output tuner settings to derive power gain contours and IMD_3 as a function of load impedance.

The measurement results for MSC88010 are shown in Figure 4.4.2 As expected, the load impedance for best power gain at high level and for optimum intermodulation performance is relatively close to center of the Smith chart.

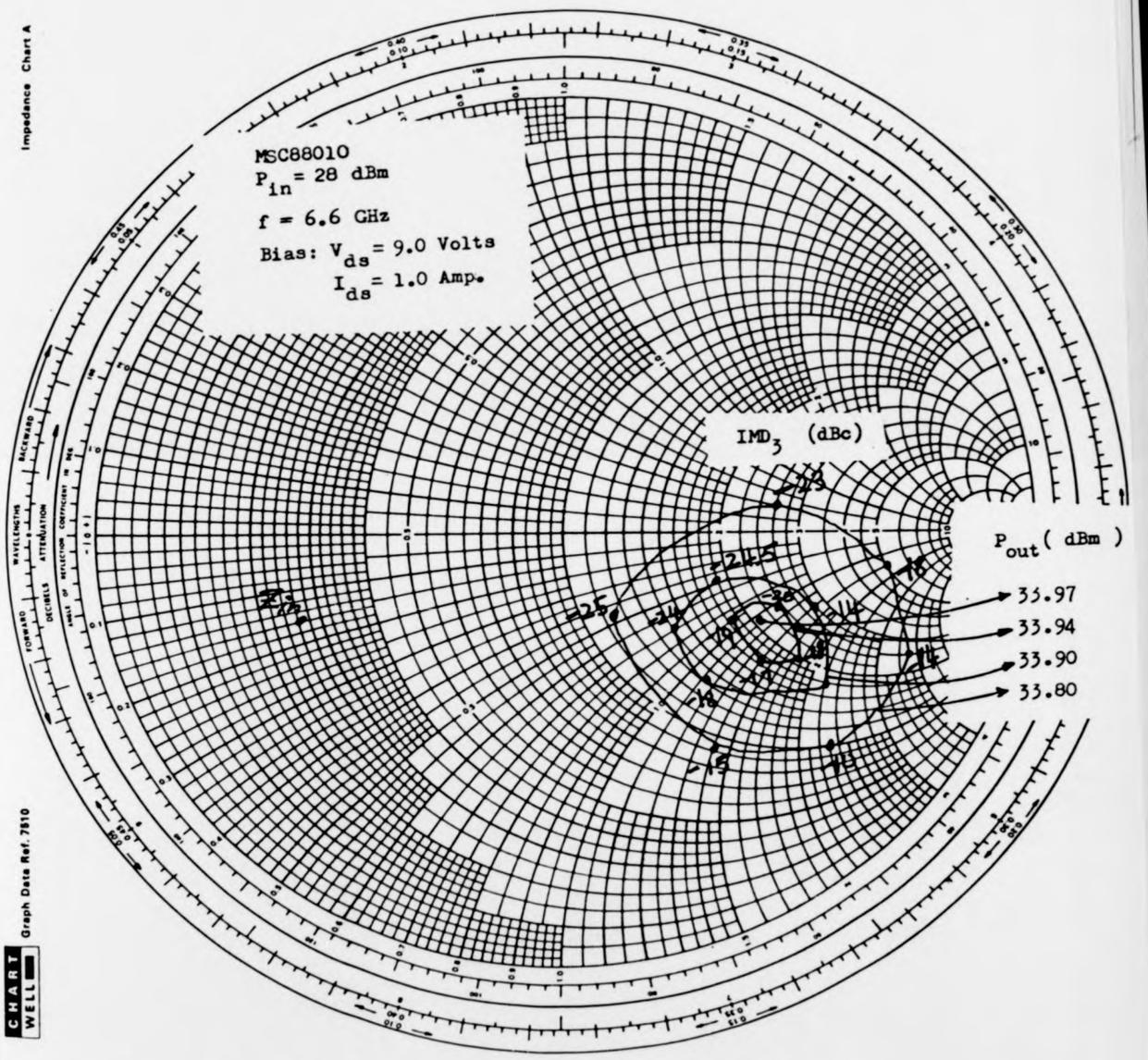


Figure 4.4.2 Load-Impedance Contours for Constant Output Power and Third-Order Intermodulation Distortion IMD_3 of the MSC88010

4.5 References

1. Matthaei,G.L.,Young,L.,Jones,E.M.T.:" Microwave Filters, Impedance-Matching Networks, and Coupling Structures," McGraw-Hill,1964, pp. 120-130.
2. Ha,Tri T.:" Solid-State Microwave Amplifier Design," Jone Wiley & Son, 1981,pp.203-209.
3. Youichi,A. et al.:" High Power GaAs FET Amplifier for TWT Replacement," Fujitsu Scientific & Technical Journal, September 1979,pp. 63-82.
4. Cusack,J. et al.:" Automatic Load Countour Mapping for Microwave Power Transistors," IEEE MTT-24,No.12,pp.1146-1152(December 1974).
5. Takayama,Y.:"A New Load-Pull Characterization Method for Microwave Power Transistors," 1976 IEEE MTT-S,June 1976,pp.218-220.
6. Kelly W. et al.:" Design of Linear GaAs FET Amplifier," Conference Proceedings of the 7th European Microwave Conference, September 1977,pp. 105-109.
7. Stancliff,R. et al.:" Harmonic Load Pull," 1976 IEEE MTT-S, June 1976,pp.185.
8. Zemack,D.:" A New Load Pull Measurement Technique Eases GaAs Charaterization," Microwave Journal, November 1980,pp. 63-67.
9. de Koning,J.G. et al.:" Spot Compression Points with Equal-Gain Circles," Microwaves ,October 1977,pp.60-77.

CHAPTER 5 A COMPLETE DESIGN FOR AN 8 GHz, 10 WATT SOLID STATE POWER AMPLIFIER FOR TWT REPLACEMENT

5.1 AN 8 GHz, 10 WATT SOLID-STATE POWER AMPLIFIER DESIGN REQUIREMENT

The RD-3 is Northern Telecom's long-haul (6560 km) digital microwave radio system, capable of transmitting and receiving a single bit stream of 91.04 Mbit/s RF channel, giving it a capacity of 1344 VF channels. There are 12 RF channels operating in the 7.725-8.275 GHz common carrier band(1)(2). This digital radio has been in service since 1978 using a 10 W TWT amplifier in the transmitter.

5.1.1 SPECIFICATION

In order to replace the TWT by solid state power amplifier, the following specification must be met.

Frequency range:	7.725 - 8.275 GHz (550 MHz Bandwidth)
Input power level: (Nominal)	-2 to 2 dBm 0 dBm
Output power level:	30- to 40-dBm continuously adjustable
Small Signal Gain:	52 $\pm$ 2 dB
Gain ripple (max):	$\pm$ 2 dB
Gain slope (max):	.3 dB/25MHz
Input return loss:	20 dB min
Output return loss: (with isolator)	20 dB min
AM/PM conversion factor:	2° /dB max
AM/AM conversion factor:	.8 dB/dB max
Group delay response:	10 ns/ 20 MHz
Noise figure:	10 dB max
Operating temperature:	0° to 50° C
Harmonic output:	-35 dBc
MTBF (at 26° C):	200,000 hrs. min
Output power variation with temperature:	$\pm$ 1.5 dB

5.2 POWER AMPLIFIER LINE-UP AND GAIN BUDGET

The power amplifier line-up and gain budget is shown in Figure 5.2.1.

There are five modules in the amplifier, each module is isolated either by drop-in isolator or 3-dB branch-line coupler.

In order to control the linearity of the amplifier, the number of stages of each module is limited to two.

Microstrip circuits are fabricated on 25 X 10^{-3} in-thick Duroid substrate with a relative dielectric constant of 10.2.

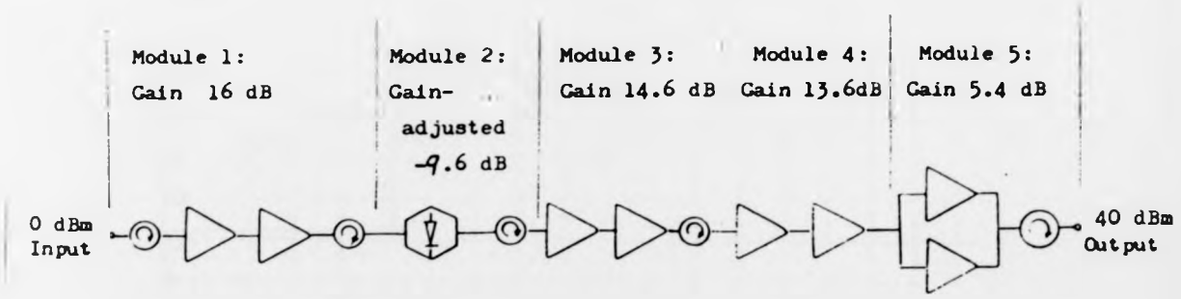


Figure 5.2.1 (a) Block Diagram for Seven-stage 10 W Solid-state Power Amplifier

(With PIN diode Gain adjusted (offset) to -9.6 dB)

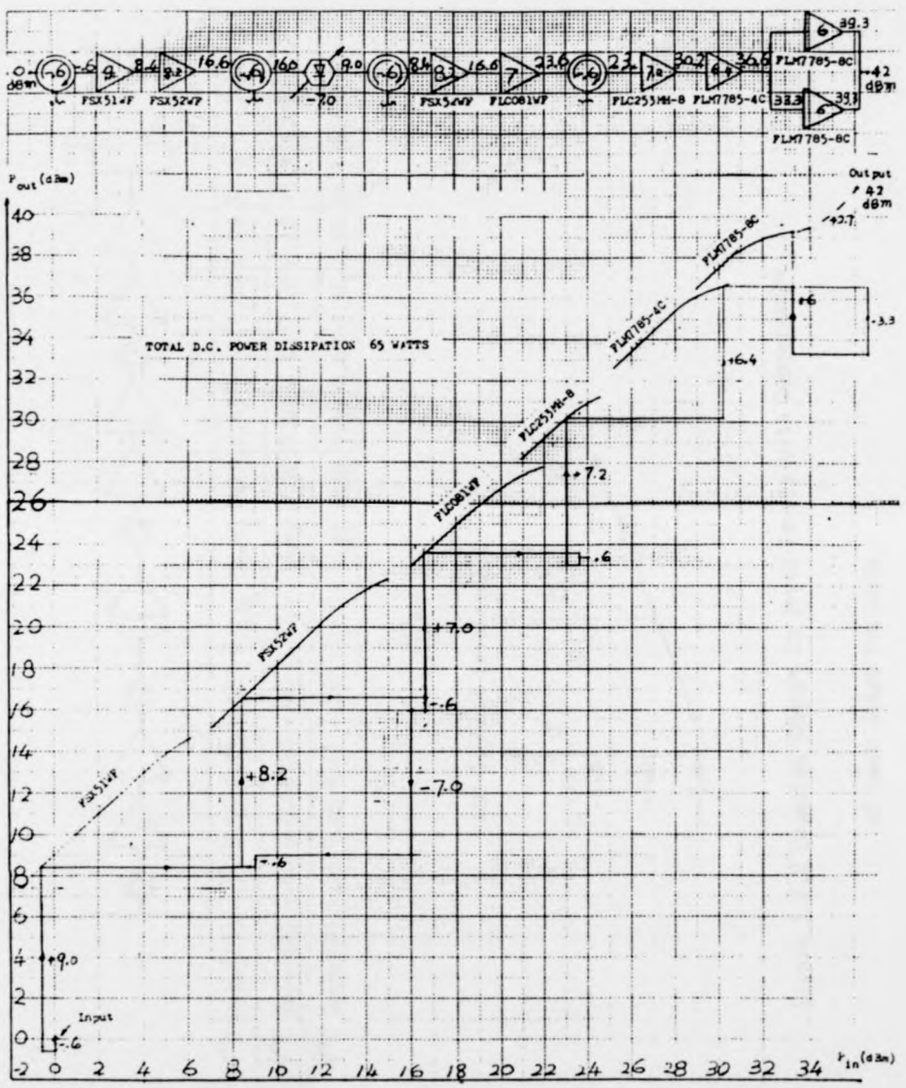
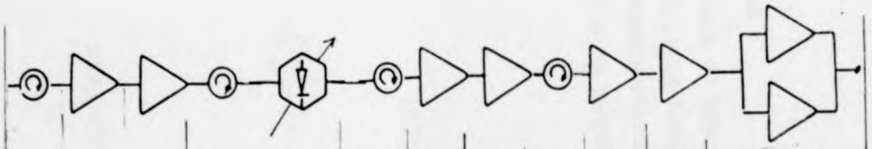


Figure 5.2.1 8 GHz, 10 Watt SSPA Line-Up and Gain Budget



50°C Gain(dB)	-.55	8.55	7.79	-.55	-4.6	-.55	7.79	6.65	-.55	6.84	6.08	-3.3	5.7	2.7
25°C Gain(dB)	-.60	9.00	8.20	-.60	-7.0	-.60	8.20	7.00	-.60	7.20	6.40	-3.3	6.0	2.7
0°C Gain(dB)	-.65	9.45	8.61	-.65	-9.4	-.65	8.61	7.35	-.65	7.56	6.72	-3.3	6.3	2.7

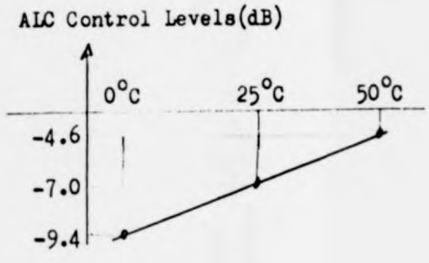


Figure 5.2.2 Expected Change in Power Levels with Temperature of Each Stage for SSPA

5.3 MODULE 1

Based on the design principles described in Chapters 3 & 4, using commercially available software package: Super COMPACT, with typical S-parameters given by manufacturers, module 1 as shown in Figure 5.3.1 is developed. Fujitsu FSX51WF and FSX52WF devices are used.

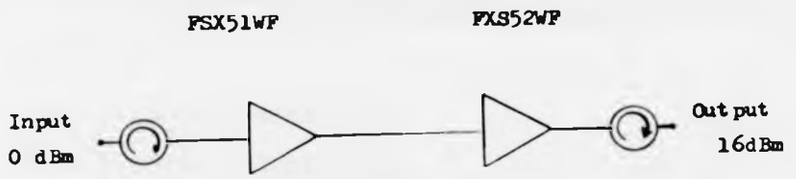


Figure5.3.1 Module 1

Table 5.3.1 is the SUPER-COMPACT data file of module 1 and Table 5.3.2 contains the theoretical results.

Figure 5.3.2 shows the MIC schematic of module 1.

Table 5.3.1 Super-Compact data file of module 1

```
BLK
   TEE 4 5 6 W1=24MIL W2=24MIL W3=8MIL SUB
   TRL 6 7 W=8MIL P=145MIL SUB
   STEP 7 8 W1=8MIL W2=80MIL SUB
   TRL 8 9 W=80MIL P=125MIL SUB
   RES 9  R=1.0E+7
   SRC 8 0 R=50 C=82PF
   BIAS: 2POR 4 5
   END
LAD
TRL 1 2 W=24MIL P=120MIL SUB
C: SLC 2 3 L=0.31NH C=1.3PF
TRL 3 4 W=24MIL P=20MIL SUB
BIAS 4 5
TRL 5 6 W=24MIL P=160MIL SUB
*STEP 6 7 W1=24MIL W2=80MIL SUB
TRL 6 8 W=?78.462MIL? P=?145.62MIL? SUB
TWO 8 9 Q1
TRL 9 10 W=24MIL P=20MIL SUB
* STEP 10 11 W1=24MIL W2=190MIL SUB
X:TRL 10 12 W=?23.853MIL? P=?3.0067MIL? SUB
BIAS 12 13
X 13 14
C 14 15
TRL 15 16 W=24MIL P=40MIL SUB
BIAS 16 17
TRL 17 18 W=24MIL P=10MIL SUB
OST 18 20 W=110MIL P=?70.67MIL? SUB
TRL 20 21 W=24MIL P=30MIL SUB
OST 21 22 W=40MIL P=?57.051MIL? SUB
TRL 22 23 W=24MIL P=50MIL SUB
TWO 23 24 Q2
TRL 24 25 W=24MIL P=?79.34MIL? SUB
*STEP 25 26 W1=24MIL W2=112MIL SUB
TRL 25 27 W=?108.57MIL? P=?52.036MIL? SUB
*STEP 27 28 W1=112MIL W2=24MIL SUB
TRL 27 29 W=24MIL P=140MIL SUB
BIAS 29 30
TRL 30 31 W=24MIL P=20MIL SUB
C 31 32
TRL 32 33 W=24MIL P=120MIL SUB
MOD1:2POR 1 33
END
   FREQ
   STEP 7.7GHZ 8.3GHZ .1GHZ
   END
   OUT
   PRI MOD1 S
   END
DATA
SUB: MS H=25.0MIL ER=10.2 MET1=CU 1.4MIL TAND=0.0020
Q1: FUJBB
Q2: FUJCC
END
```

```
OPT
MOD1 R1=50 R2=50
F=7.7GHZ 7.8GHZ MS21=19DB GT W=5  MS22=.15 LT
F=7.9GHZ 8.1GHZ MS21=16DB LT W=5 MS22=1.5 LT
F=8.2GHZ 8.3GHZ MS21=19Db GT W=5 MS22=1.5 LT
END
```

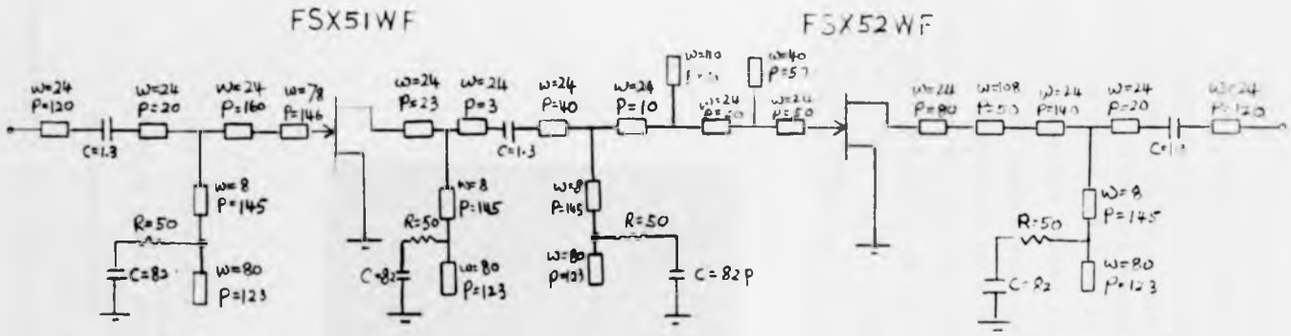
```
FILE: OPT1      DATA


 SUPER-COMPACT  Version 1.6+158  5/16/83       22:12:03  05/29/84


 CIRCUIT:  MOD1       FILENAME "MOD1OPT1"
 S-MATRIX, ZS =    50.0+J    0.0  ZL =    50.0+J    0.0

   FREQ          S11             S21             S12             S22          S21    STAB SGN
    GHZ       MAG     ANG     MAG     ANG     MAG     ANG     MAG     ANG     dB       K  B1
   7.70000   0.170     55   6.895    -122   0.004     166   0.291     137   16.77   17.10 +
   7.80000   0.132     13   7.952    -149   0.005     140   0.216     103   18.01   13.11 +
   7.90000   0.127    -38   8.719    -178   0.005     111   0.167      51   18.81   10.77 +
   8.00000   0.145    -79   8.896     152   0.005      82   0.179      -6   18.98    9.91 +
   8.10000   0.164   -107   8.465     123   0.005      53   0.221     -45   18.55   10.35 +
   8.20000   0.177   -125   7.688      96   0.005      27   0.255     -69   17.72   11.90 +
   8.30000   0.190   -137   6.832      72   0.005       3   0.275     -86   16.69   14.37 +
```

Table 5.3.2 Super-Compact analysis results for module 1



where w: the width of microstrip line in MILs

p: the physical length of microstrip line in MILs

R: the value of resistor in Ohms

C: the value of capacitor in pF.

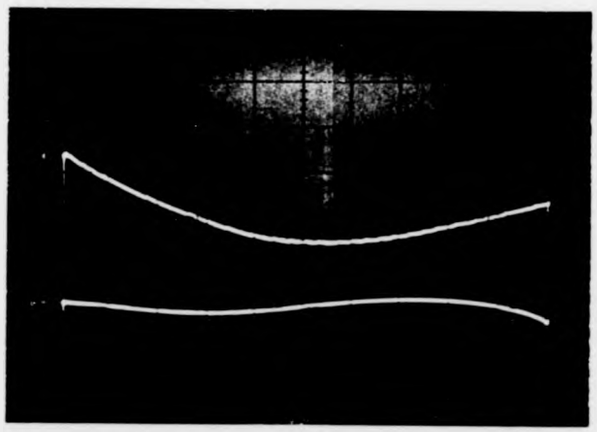
Figure 5.3.2 Schematic of two-stage linear amplifier of Module 1.

5.3.2 Module 1 Measurement Results

The module 1 Delta-gain and Delta-phase measurements are made utilising the computer program developed in Chapter 2. The results are shown in Table 5.3.2.1 with bias voltages set such that I_{ds} is equal to half of I_{dss} for both transistors (3).

From Table 5.3.2.1, it is noted that the overall gain is higher than the expected value, for example: the small signal gain is 23.36 dB (about 5 dB higher than design value) at 7.7 GHz, and the output power is compressed by 1.8 dB at 0 dBm input power, it is not desirable. By reducing the I_{ds} from 30 ma to 15 ma for the first stage transistor and from 75 ma to 50 ma for the second stage of the transistor, the optimized performance is then obtained as shown in Table 5.3.2.2, after fine tuning.

Figure 5.3.2.1 shows the gain response and input return loss of module 1.



Top trace: Gain response, Vertical scale: 1 dB/Div.
Reference at center line is 17 dB.
Bottom trace: Input return loss , Vertical scale 10 dB/Div.
Reference at center line is 0 dB.
Horizontal scale for both traces: 60 MHz/Div.
Left edge is 7.7 GHz, right edge is 8.3 GHz.

Figure 5.3.2.1 The Gain response and Input Return Loss of Module 1

01:19:45
FREQ (GHz) = 7.7 GAIN (dB) = 23.36

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
-10.00	13.36	0.00	0.00
-9.00	14.30	-.06	.09
-8.00	15.23	-.13	.16
-7.00	16.13	-.23	.34
-6.00	17.01	-.35	.46
-5.00	17.86	-.50	.71
-4.00	18.67	-.69	.96
-3.00	19.45	-.91	1.13
-2.00	20.20	-1.16	1.44
-1.00	20.92	-1.44	1.91
0.00	21.56	-1.80	2.39
1.00	22.19	-2.17	3.03
2.00	22.77	-2.59	3.76

01:19:58
FREQ (GHz) = 8 GAIN (dB) = 20.83

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
-10.00	10.83	0.00	0.00
-9.00	11.82	-.01	.07
-8.00	12.79	-.04	.26
-7.00	13.73	-.10	.47
-6.00	14.69	-.14	.66
-5.00	15.60	-.23	.84
-4.00	16.52	-.31	1.10
-3.00	17.40	-.43	1.46
-2.00	18.28	-.55	1.64
-1.00	19.10	-.73	2.20
0.00	19.90	-.93	2.69
1.00	20.64	-1.19	3.21
2.00	21.36	-1.47	3.97

01:20:11
FREQ (GHz) = 8.3 GAIN (dB) = 21.76

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
-10.00	11.76	0.00	0.00
-9.00	12.73	-.03	.21
-8.00	13.69	-.07	.51
-7.00	14.63	-.13	.83
-6.00	15.55	-.21	1.14
-5.00	16.46	-.30	1.60
-4.00	17.33	-.43	2.09
-3.00	18.21	-.55	2.64
-2.00	19.07	-.69	3.33
-1.00	19.88	-.88	4.07
0.00	20.66	-1.10	5.14
1.00	21.40	-1.36	6.19
2.00	22.10	-1.66	7.51

Table:5.3.2.1 Module 1 Delta-gain and Delta-phase measurement results (before optimum biasing)

Table 5.3.2.2 Module 1 delta-gain and delta-phase measurement results

Module #1 with Fsx51 Bias Inf 08:45:51 (after optimum biasing)

FREQ (GHz) = 7.7 GAIN (dB) = 18.49

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)
-10.00	8.89	0.00	0.00	-1.19	-1550.00	15.58	9.11
-9.00	9.88	-.01	-.11	-2.38	-1550.00	15.64	9.10
-8.00	10.89	0.00	-.16	-1.19	-1550.00	15.73	9.10
-7.00	11.88	-.01	-.20	-4.76	-1550.00	15.83	9.09
-6.00	12.89	0.00	-.30	-4.76	-1550.00	15.98	9.07
-5.00	13.89	0.00	-.37	-4.76	-1550.00	16.13	9.06
-4.00	14.87	-.02	-.46	-4.76	-1550.00	16.28	9.05
-3.00	15.85	-.04	-.46	-7.14	-1550.00	16.49	9.03
-2.00	16.83	-.06	-.46	-4.76	-1550.00	16.71	9.01
-1.00	17.78	-.11	-.54	-8.33	-1550.00	16.98	8.99
0.00	18.71	-.18	-.57	-8.33	-1550.00	17.29	8.96
1.00	19.59	-.30	-.61	-8.33	-1550.00	17.65	8.93
2.00	20.42	-.47	-.64	-8.33	-1550.00	18.08	8.89

FREQ (GHz) = 8 GAIN (dB) = 16.47

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)
-10.00	6.07	0.00	0.00	0.00	-1550.00	15.61	9.11
-9.00	7.07	0.00	-.11	-1.19	-1550.00	15.67	9.10
-8.00	8.10	.03	-.17	-1.19	-1550.00	15.73	9.09
-7.00	9.10	.03	-.24	-1.19	-1550.00	15.85	9.09
-6.00	10.12	.05	-.31	-1.19	-1550.00	15.98	9.07
-5.00	11.13	.06	-.47	-1.19	-1550.00	16.12	9.06
-4.00	12.15	.08	-.41	0.00	-1550.00	16.28	9.05
-3.00	13.17	.10	-.53	-1.19	-1550.00	16.43	9.03
-2.00	14.18	.11	-.61	-1.19	-1550.00	16.65	9.01
-1.00	15.18	.11	-.66	-2.38	-1550.00	16.89	8.99
0.00	16.16	.09	-.76	-2.38	-1550.00	17.16	8.97
1.00	17.16	.09	-.91	-1.19	-1550.00	17.47	8.94
2.00	18.12	.05	-.89	-4.76	-1550.00	17.84	8.91

FREQ (GHz) = 8.3 GAIN (dB) = 17.43

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)
-10.00	7.73	0.00	0.00	-2.38	-1550.00	15.67	9.10
-9.00	8.74	.01	-.09	-1.19	-1550.00	15.76	9.09
-8.00	9.74	.01	-.19	-1.19	-1550.00	15.85	9.08
-7.00	10.76	.03	-.36	-2.38	-1550.00	16.01	9.07
-6.00	11.78	.05	-.50	-2.38	-1550.00	16.16	9.06
-5.00	12.78	.05	-.66	0.00	-1550.00	16.34	9.04
-4.00	13.79	.06	-.67	-4.76	-1550.00	16.55	9.02
-3.00	14.79	.06	-.91	-7.14	-1550.00	16.77	9.01
-2.00	15.78	.05	-.91	-3.57	-1550.00	17.01	8.98
-1.00	16.74	.01	-1.01	-8.33	-1550.00	17.29	8.96
0.00	17.69	-.04	-1.11	-3.57	-1550.00	17.62	8.93
1.00	18.61	-.12	-1.09	-8.33	-1550.00	17.99	8.90
2.00	19.51	-.22	-1.13	-5.95	-1550.00	18.38	8.86

5.4 Module 2 : PIN Diode Attenuator Module

The PIN diode is a double diffused junction with an intrinsic layer (I-layer) separating the P and N regions. At frequencies above 100 MHz, the diode ceases to be a rectifier because of carrier storage and transit time effects. Its shunt capacitance is quite small because of the separation of the P and N regions by the I-layer. Conductivity of the I-region can be varied by a dc bias current and the device becomes an electrically variable resistor which can be used for microwave attenuators up to frequencies as high as 20 GHz(6),(7).

The PIN diode attenuator as shown in Figure 5.4.1, is inserted between Module 1 and Module 3 of the amplifier. Its function is to set the overall gain of the power amplifier and to provide the control element of Automatic Levelling Circuit (ALC) for temperature compensation.

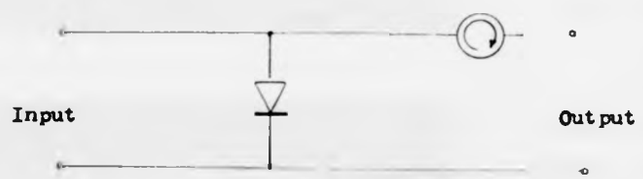
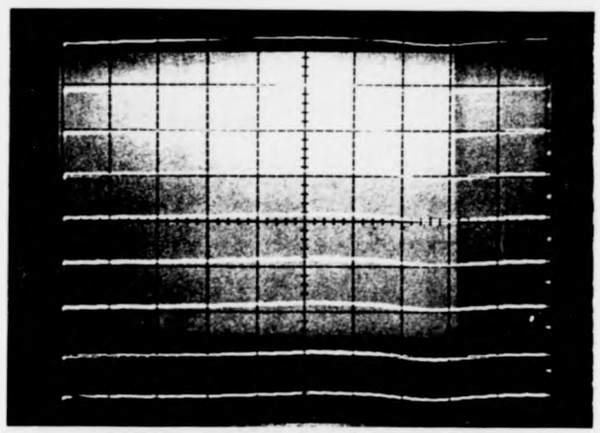
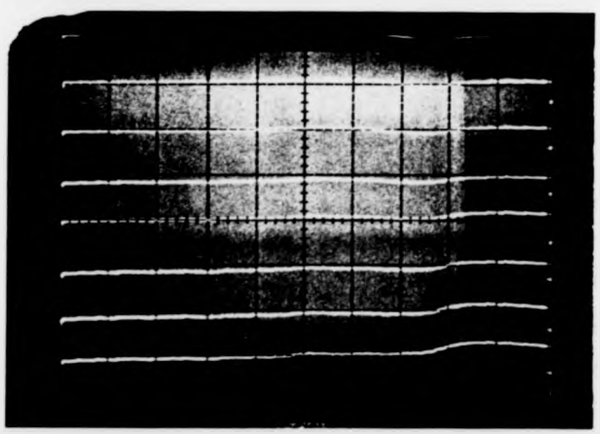


Figure 5.4.1 Module 2: PIN diode attenuator

By varying the DC current through the diode, MA47221, the attenuation can be varied by approximately 20 dB. Figure 5.4.2 is the PIN diode attenuation v.s. frequency response corresponding to the current through and voltage across the diode. To minimize interactions between the attenuator and adjacent amplifier modules, the input and output of the PIN diode are connected to microstrip drop in isolators.





	Id(ma)	Vd(V)
-2dB	0.0080	0.500
-3dB	0.0181	0.548
-4dB	0.0302	0.573
-5dB	0.0438	0.591
-6dB	0.0596	0.607
-7dB	0.0800	0.621
-8dB	0.1027	0.634
-9dB	0.1261	0.645
-10dB	0.1561	0.656
-11dB	0.1907	0.667
-12dB	0.2360	0.680
-13dB	0.2900	0.693
-14dB	0.3540	0.704
-15dB	0.4330	0.718
-16dB	0.529	0.731
-17dB	0.619	0.743
-18dB	0.703	0.786

Figure 5.4.2 Module 2: PIN diode attenuation-frequency response
Vertical scale: 1dB/div.
Horizontal scale: 60MHz/div. from 7.7 to 8.3 GHz

5.5 Mudule 3

The Module 3 is constructed using Fujitsu FSX52WF and FLC081WF as two-stage amplifier, as shown in Figure 5.5.1.

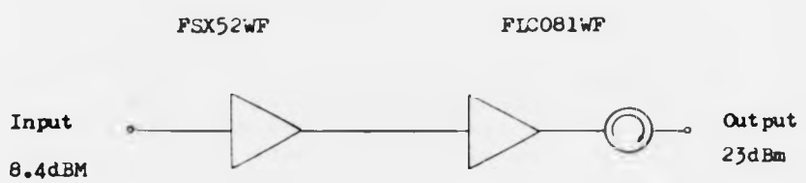


Figure 5.5.1. Module 3

Table 5.5.1 is the SUPER- COMPACT optimization data file of module 3 and Table 5.5.2 contains the theoretical results.

Figure 5.5.2 shows the MIC circuit realization on Duroid soft substrate.

Figure 5.5.3 is the gain response and input return loss of module 3.

Table 5.5.3 is the measurement results for the linearity of module 3.

Table 5.5.1 Super-Compact. data file of the Module 3.

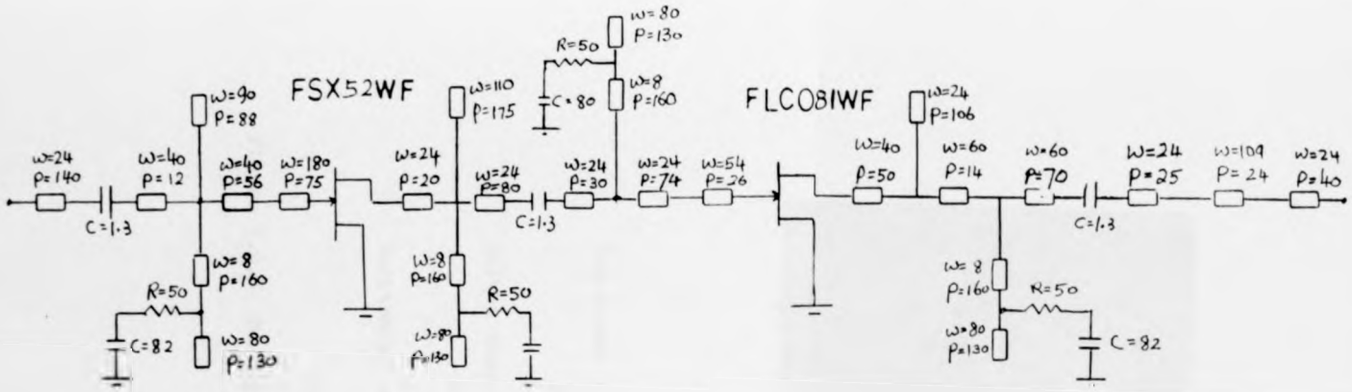
```
#X: ?109.62MIL?
#Y: ?87.826MIL?
#Z: ?109.61MIL?
BLK
    TRL 4 5 6 #1=40MIL #2=40MIL #3=8MIL SUB
    TRL 6 7 #=8MIL P=100MIL SUB
    STEP 7 8 #1=8MIL #2=60MIL SUB
    TRL 8 9 #=60MIL P=130MIL SUB
    RES 9  R=1.0E+7
    SRC 3 0 R=50 C=8.2PF
    BIAS1: ZPOL 4 5
    END
BLK
    TRL 4 5 6 #1=24MIL #2=24MIL #3=8MIL SUB
    TRL 6 7 #=8MIL P=100MIL SUB
    STEP 7 8 #1=8MIL #2=60MIL SUB
    TRL 8 9 #=60MIL P=130MIL SUB
    RES 9  R=1.0E+7
    SRC 3 0 R=50 C=8.2PF
    BIAS2: ZPOL 4 5
    END
BLK
    TRL 4 5 6 #1=60MIL #2=60MIL #3=8MIL SUB
    TRL 6 7 #=8MIL P=100MIL SUB
    STEP 7 8 #1=8MIL #2=60MIL SUB
    TRL 8 9 #=60MIL P=130MIL SUB
    RES 9  R=1.0E+7
    SRC 3 0 R=50 C=8.2PF
    BIAS3: ZPOL 4 5
    END
LAD
TRL 1 2 W=24MIL P=140MIL SUB
C: SLC 2 3 L=0.31NH C=1.3PF
TRL 3 4 W=40MIL P=12MIL SUB
OST 4 50 W=90MIL P=#Y SUB
BIAS1 50 5
TRL 5 6 W=40MIL P=56MIL SUB
STEP 6 7 #1=40MIL #2=180MIL SUB
TRL 7 8 W=180MIL P=75MIL SUB
1#0 8 9 Q1
TRL 9 10 W=24MIL P=20MIL SUB
OST 10 11 W=100MIL P=?175.01MIL? SUB
BIAS2 11 12
TRL 12 13 W=24MIL P=30MIL SUB
TRL 13 14 W=24MIL P=50MIL SUB
C 14 15
TRL 15 16 W=24MIL P=30MIL SUB
BIAS2 16 17
TRL 17 18 W=24MIL P=74MIL SUB
STEP 18 20 #1=24MIL #2=50MIL SUB
TRL 20 21 W=54MIL P=26MIL SUB
TWO 21 24 Q2
TRL 24 25 W=40MIL P=58MIL SUB
OST 25 26 W=24MIL P=#Z SUB
TRL 26 27 W=60MIL P=14MIL SUB
```

```
BIAS3 27 36
TRL 31 31 W=60MIL P=70MIL SUB
C 31 32
TRL 32 33 W=24MIL P=24.34MIL SUB
STEP 33 34 W1=24MIL W2=WX SUB
TRL 34 35 W=WX P=24MIL SUB
STEP 35 36 W1=WX W2=24MIL SUB
TRL 36 37 W=24MIL P=40MIL SUB
MOD2:PORT 1 37
END
   FREQ
   STEP 7.7GHZ 8.3GHZ 0.1GHZ
   END
   OUT
   PRI MOD2 S
END
OPT
MOD2 W1=50 W2=50
F=7.7GHZ 7.3GHZ MS21=17DB GA W=5  MS22=.2 LI
F=7.9GHZ 8.1GHZ MS21=15DB LI  MS22=.2 LI
F=8.2GHZ 8.3GHZ MS21=17DB GA W=5  MS22=.2 LI
END
DATA
SUB: ER=9.0MIL EA=10.2 NRF1=CU 1.4MIL TANL=0.0020
Q1: FUJCC
Q2:S
5GHZ .825 109 1.880 29 .054 -6 .410 -108
6GHZ .822 147 1.044 10 .054 -16 .410 -125
7GHZ .828 131 1.433 -11 .054 -25 .425 -148
8GHZ .819 119 1.250 -29 .054 -36 .439 -165
9GHZ .805 107 1.091 -50 .055 -46 .460 176
END
```

S-MATRIX, ZS = 50.0+J 0.0 ZL = 50.0+J 0.0

FREQ	S11		S21		S12		S22		S21	STAB	SGN
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	dB	K	B1
7.70000	0.243	-108	5.150	-87	0.006	-134	0.192	21	14.24	15.14	+
7.80000	0.147	-148	5.901	-109	0.007	-155	0.142	-9	15.42	11.84	+
7.90000	0.125	130	6.602	-135	0.008	180	0.119	-56	16.39	9.29	+
8.00000	0.232	71	7.009	-164	0.009	152	0.141	-106	16.91	7.64	+
8.10000	0.349	39	6.889	167	0.009	124	0.182	-140	16.76	7.01	+
8.20000	0.428	14	6.285	139	0.008	97	0.214	-163	15.97	7.48	+
8.30000	0.465	-4	5.462	113	0.007	72	0.231	-178	14.75	9.13	+

Table 5.2.2 Supercompact Analysis of the Moduole 3



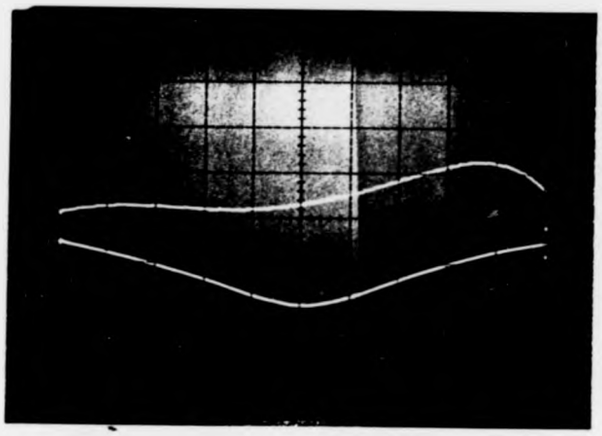
where w: the width of microstrip line in MILS

p: the physical length of microstrip line in MILS

R: the value of resistor in Ohms

C: the value of capacitor in pF.

Figure 5.5.2 Schematic of two-stage linear amplifier of Module 3.



Top trace: Gain response
Vertical scale: 1 dB/ Div.
refefence at center line is 15 dB
Bottom trace: Input return loss
Vertical scale: 10 dB/ Div.
reference at center line is 0 dB
Horizontal scale : 60 MHz/ Div.
Left edge is 7.7 GHz;
Right edge is 8.3 GHz

Figure 5.5.3 The Gain and Input Return Loss of the Module 3.

Table 5.5.3 The Linearity measurement Results of the Module 3
(Gate current & gate voltage of the FLC081WF is measured)

FREQ (GHz) = 7.7 GAIN (dB) = 14.99

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)
0.00	14.99	0.00	0.00	-25.00	-2520.00
1.00	15.98	-.01	.26	-33.33	-2520.00
2.00	16.95	-.04	.38	-40.00	-2520.00
3.00	17.90	-.09	.42	-50.00	-2515.00
4.00	18.85	-.14	.54	-66.67	-2510.00
5.00	19.78	-.21	.72	-91.67	-2505.00
6.00	20.68	-.31	.98	-140.00	-2495.00
7.00	21.56	-.43	1.32	-223.33	-2475.00
8.00	22.39	-.60	1.72	-331.67	-2449.00
9.00	23.10	-.89	1.92	-465.00	-2416.00
10.00	23.61	-1.38	1.86	-601.67	-2385.00
11.00	24.01	-1.98	1.88	-743.33	-2350.00

FREQ (GHz) = 8 GAIN (dB) = 14.51

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)
0.00	14.51	0.00	0.00	-8.33	-2525.00
1.00	15.51	0.00	0.00	-8.33	-2525.00
2.00	16.49	-.02	.18	-8.33	-2525.00
3.00	17.49	-.02	.38	-13.33	-2525.00
4.00	18.47	-.04	.62	-16.67	-2525.00
5.00	19.48	-.03	.92	-16.67	-2525.00
6.00	20.45	-.06	1.24	-16.67	-2525.00
7.00	21.43	-.08	1.54	-18.33	-2523.00
8.00	22.36	-.15	1.86	-25.00	-2520.00
9.00	23.27	-.24	2.38	-25.00	-2520.00
10.00	24.15	-.36	2.74	-33.33	-2520.00
11.00	24.96	-.55	3.24	-41.67	-2520.00

FREQ (GHz) = 8.3 GAIN (dB) = 15

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)
0.00	15.00	0.00	0.00	-16.67	-2525.00
1.00	15.97	-.03	-.06	-16.67	-2525.00
2.00	16.97	-.03	.20	-25.00	-2520.00
3.00	17.95	-.05	.14	-25.00	-2520.00
4.00	18.95	-.05	.04	-33.33	-2520.00
5.00	19.94	-.06	.12	-41.67	-2515.00
6.00	20.88	-.12	0.00	-58.33	-2515.00
7.00	21.80	-.20	.04	-78.33	-2510.00
8.00	22.68	-.32	-.02	-116.67	-2500.00
9.00	23.50	-.50	-.28	-183.33	-2485.00
10.00	24.24	-.76	-.46	-300.00	-2455.00
11.00	24.83	-1.17	-.98	-463.33	-2419.00

5.6 Module 4

Figure 5.6.1 shows module 4 of two stage amplifier, using Fujitsu FLC253MH-8 and FLM7785-4C devices.

Figure 5.6.1 Module 4

Since FLM7785-4C is internally matched device in 50 ohms system, the design of first stage: FLC253MH-8, is optimized by using Super-Compact and the data file is shown in Table 5.6.1.

Figure 5.6.2 is the schematic of two-stage linear amplifier of module 4.

Figure 5.6.3 is the gain response and input return loss of module 4, and Figure 5.6.4 is the output return loss of module 4.

Table 5.6.3 is the measurement results for the linearity of module 4.

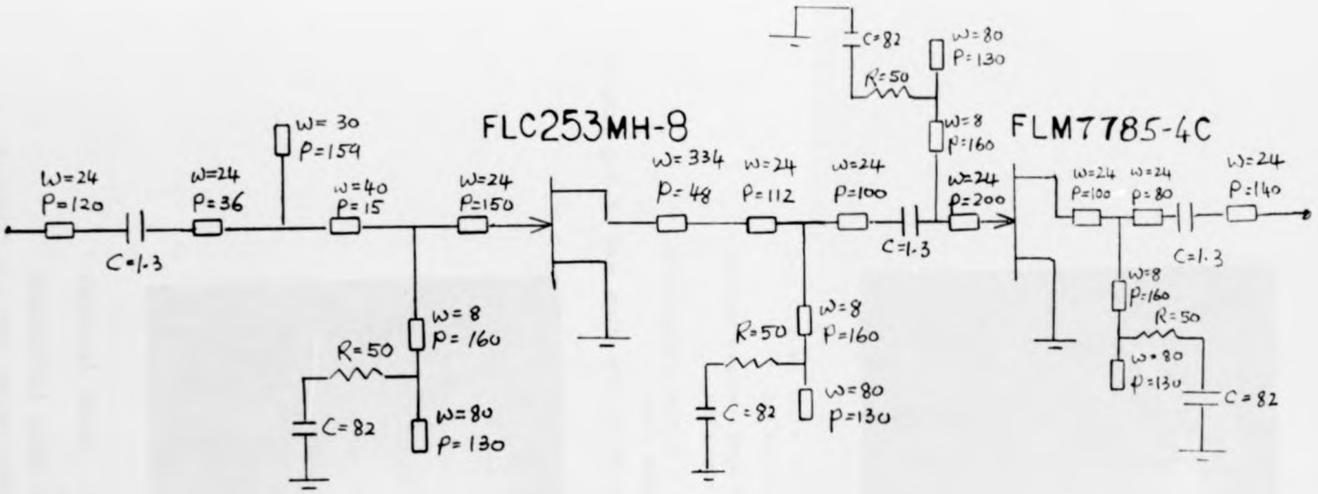
Table 5.6.1 SUPERCOMPACT Data File for The First Stage of the Module 4

```
WX: ? 159.07MIL?
WY: ? 333.95MIL?
BLK
   TRL 4 5 6 W1=60MIL W2=60MIL W3=6MIL SUB
   TRL 6 7 W=6MIL P=100MIL SUB
   STEP 7 8 W1=6MIL W2=60MIL SUB
   TRL 8 9 W=60MIL P=150MIL SUB
   RLS 9  R=1.0E+7
   SHC 8 0 R=50 C=.22PF
   BIAS: ZPOR 4 5
   END
LAD
TRL 1 2 W=24MIL P=120MIL SUB
C: SLC 2 3 L=0.31NH C=1.3PF
TRL 3 4 W=24MIL P=30MIL SUB
OST 4 40 W=30MIL P=WX SUB
TRL 40 41 W=24MIL P=15MIL SUB
BIAS 41 5
TRL 5 6 W=24MIL P=150MIL SUB
TWO 6 9 21
TRL 9 10 W=WY P=48MIL SUB
STEP 10 11 W1=WY W2=24MIL SUB
TRL 11 12 W=24MIL P=112MIL SUB
BIAS 12 13
TRL 13 14 W=24MIL P=100MIL SUB
C 14 15
TRL 15 16 W=24MIL P=30MIL SUB
MOD4: ZPOR 1 16
   END
FREQ
STEP 7.6GHZ 8.4GHZ .1GHZ
END
   OUT
   PRI MOD4 S
END
OPT
MOD4 R1=50 R2=50
P=7.7GHZ 7.9GHZ MS21=9DB GT W=5  MS22=.2 LT
P=7.9GHZ 8.1GHZ MS21=7DB LT  MS22=.2 LT
P=8.2GHZ 8.3GHZ MS21=9DB GT W=5  MS22=.2 LT
END
DATA
SUB: MS H=25.0MIL ER=10.2 MET1=CU 1.4MIL TAND=0.0020
Q1:S
7.6GHZ .568 55.3 1.353 -83.5 .038 -98.9 .829 171.2
7.8GHZ .503 45.7 1.406 -91.7 .039 -111. .852 168.7
8.0GHZ .419 34.7 1.471 -102.3 .042 -124.3 .866 166.1
8.2GHZ .307 22.8 1.514 -116.5 .046 -139. .872 161.1
8.4GHZ .194 12.6 1.512 -127.5 .048 -151.5 .871 155.6
END
```

CIRCUIT: BOI4
S-MATRIX, ZS = 50.0+J 0.0 ZL = 50.0+J 0.0

FREQ	S11		S21		S12		S22		S21	STAB	SGN
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG	dB	K	B1
7.60000	0.670	15	1.983	-116	0.056	-131	0.561	-137	5.95	1.93	+
7.70000	0.661	-2	2.159	-130	0.060	-147	0.528	-146	6.69	1.86	+
7.80000	0.654	-20	2.317	-144	0.064	-164	0.477	-155	7.30	1.77	+
7.90000	0.645	-38	2.463	-160	0.069	180	0.422	-163	7.83	1.70	+
8.00000	0.631	-56	2.613	-177	0.075	161	0.344	-169	8.34	1.65	+
8.10000	0.598	-79	2.745	161	0.081	138	0.238	-164	8.77	1.62	+
8.20000	0.538	-102	2.791	137	0.085	114	0.203	-132	8.92	1.62	+
8.29999	0.457	-123	2.712	113	0.085	90	0.309	-115	8.67	1.65	+
8.40000	0.373	-141	2.540	93	0.081	69	0.435	-119	8.10	1.73	+

Table 5.6.2 SUPERCOMPACT Analysis for the First stage of the Module 4



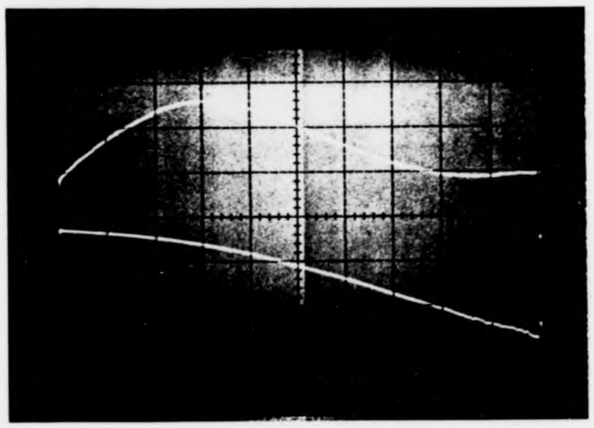
where w: the width of microstrip line in MILS

p: the physical length of microstrip line in MILS

R: the value of resistor in Ohms

C: the value of capacitor in pF.

Figure 5.6.2 Schematic of two-stage linear amplifier of Module 4

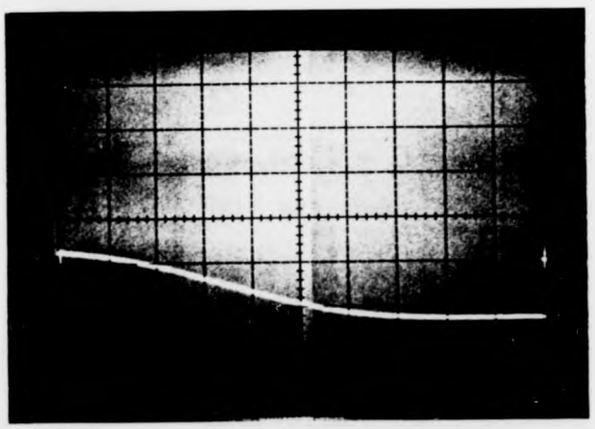


Top trace: Gain response, vertical scale 1 dB/Div.
Reference at center line is 15 dB.

Bottom trace: Input return loss, vertical scale 10 dB/Div.
Reference at center line is 0 dB.

Horizontal scale : 60 MHz / Div.
Left edge is 7.7 GHz, right edge is 8.3 GHz.

Figure 5.6.3 The gain and Input return loss of Module 4.



Vertical scale : 10 dB/Div.,the center line represents 0 db reference.
Horizontal scale is the same scale as in Figure 5.6.3.

Figure 5.6.4 The output return loss of the Module 4.

Table 5.6.3 The linearity measurement results of the module 4

FREQ (GHz) = 7.7 GAIN (dB) = 14.72

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
14.00	28.72	0.00	0.00
15.00	29.74	.02	.36
16.00	30.78	.06	.72
17.00	31.83	.11	1.20
18.00	32.83	.11	1.62
19.00	33.76	.04	1.72
20.00	34.60	-.12	1.82
21.00	35.35	-.37	2.22
22.00	35.95	-.77	5.00
23.00	36.41	-1.31	11.58
24.00	36.60	-2.12	22.20

FREQ (GHz) = 8 GAIN (dB) = 13.61

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
14.00	27.61	0.00	0.00
15.00	28.63	.02	.24
16.00	29.66	.05	.62
17.00	30.68	.07	.98
18.00	31.67	.06	1.40
19.00	32.67	.06	1.88
20.00	33.56	-.05	2.22
21.00	34.37	-.24	2.54
22.00	34.98	-.63	2.68
23.00	35.47	-1.14	2.90
24.00	35.95	-1.66	3.46

FREQ (GHz) = 8.3 GAIN (dB) = 15.42

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
14.00	29.42	0.00	0.00
15.00	30.42	0.00	.32
16.00	31.44	.02	.74
17.00	32.43	.01	1.32
18.00	33.38	-.04	1.78
19.00	34.22	-.20	2.20
20.00	34.92	-.50	2.30
21.00	35.45	-.97	2.68
22.00	35.86	-1.56	3.58
23.00	36.20	-2.22	5.24
24.00	36.43	-2.99	7.18

5.7 Module 5

Figure 5.7.1 is the balanced amplifier(7)-(11), using two FLM7785-8C internally matched power devices.

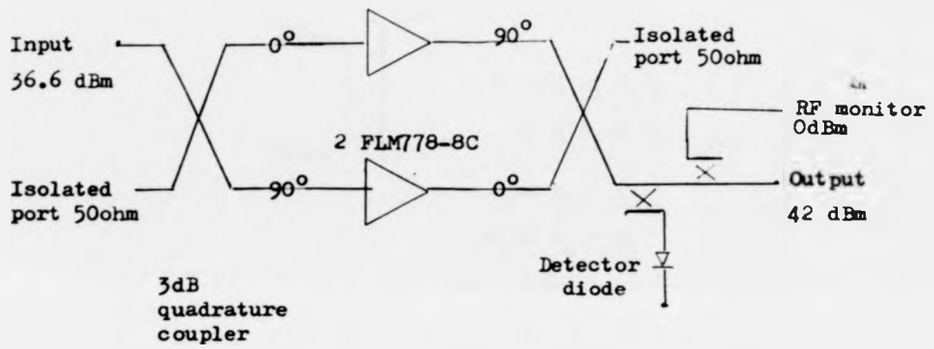


Figure 5.7.1 Module 5 balanced amplifier

Module 5 consists of two 3-dB quadrature couplers, one 40 dB coupler for monitoring the output of the amplifier and the other 40 dB coupler in conjunction with detector diode as an important element for Automatic Level Control (ALC) circuit.

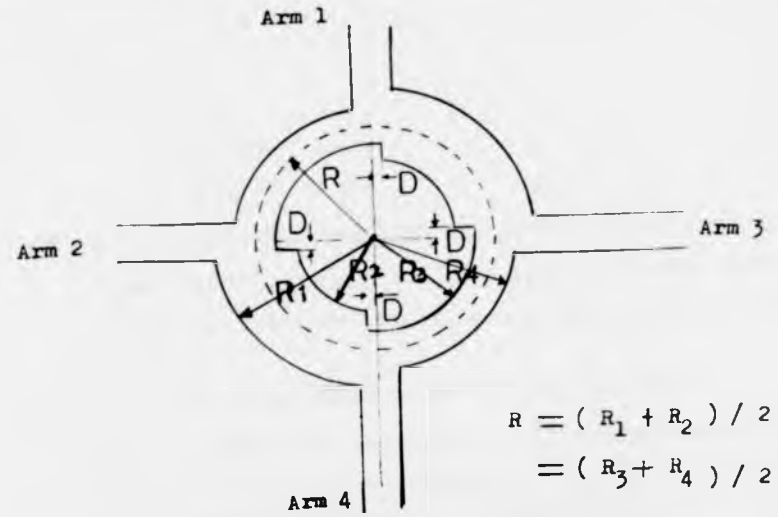
5.7.1 3-dB Quadrature coupler

A design of 3-dB branch line coupler is well-known(12). In order to achieve a good performance for this kind of coupler, using the following method of the author which has been found very useful.

As shown in Figure 5.7.1.1. By solving the two Eqns. (5.7.1.1) and (5.7.1.2):

$$\pi R - 4D = \frac{\lambda_{35}}{2} \qquad (5.7.1.1)$$

$$\pi R + 4D = \frac{\lambda_{50}}{2} \qquad (5.7.1.2)$$



$$R = (R_1 + R_2) / 2$$
$$= (R_3 + R_4) / 2$$
$$W_2 = R_1 - R_2$$
$$W_1 = R_4 - R_3$$

Figure 5.7.1.1 3-dB branch line coupler

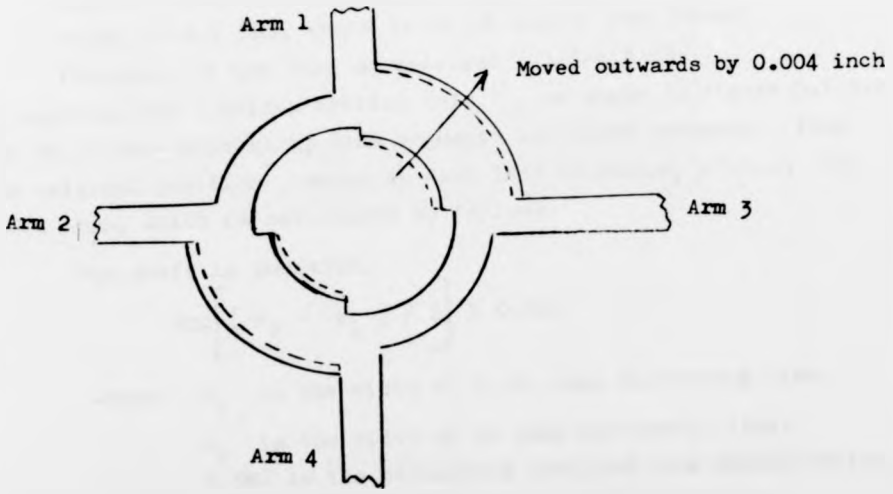


Figure 5.7.1.2 3-dB branch line coupler after optimization

Yield

R = 0.0877 inch

D = 0.0010 inch

Where λ_{50} is the wavelength of the 50 ohms line, which is obtained from COMPACT as equal to 0.543 inch on Luroid substrate with 0.025 inch thickness having a relative dielectric constant of 10.2.

λ_{35} is the wavelength of the 35.35 ohms line.

R is the radius of the circle with circumference equal to the sum of the half-wavelength of the 50 ohms line (λ_{50} / 2) and the half-wavelength of the 35.35 ohms line (λ_{35} / 2).

4D is the difference between the two half-wavelengths.

See Figure 5.7.1.1.

The optimization is done by only one iteration using Golden-ratio(13) search on the 35.35 ohms microstrip line segments, at frequency equal to 8.1 GHz, which is 12.5% higher than center frequency of the band of interest (7.7-8.3 GHz).

By applying the " Golden Section Rule " , as shown in Figure 5.7.1.2, the 35.35 ohms microstrip line segments are moved outwards from the original position , shown in dash-line of Figure 5.7.1.2, by 0.004 inch, which is calculated as follows:

The shift in position,

$$x = \left[(W_2 - W_1) / 2 \right] \times 0.382$$

where W_2 is the width of 35.35 ohms microstrip line.

W_1 is the width of 50 ohms microstrip line.

0.382 is the correction obtained from Golden-section rule .

The performance of 3-dB coupler after optimization, including biasing network are shown in Figures 5.7.1.3 to 5.7.1.5.

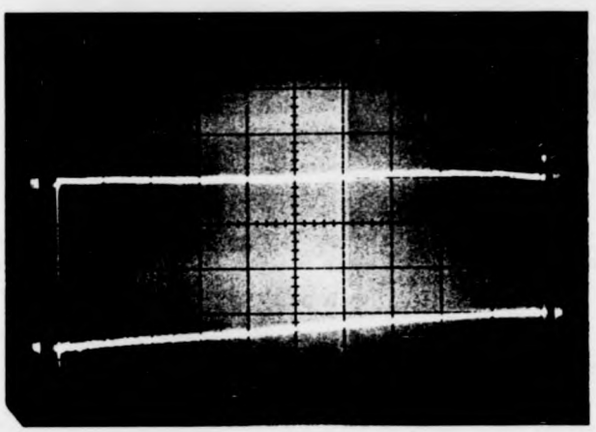


Figure 5.7.1.3 Amplitude and input return loss between arm 1 and arm 3.

Top trace: Amplitude response:
Vertical scale: 1 dB/Div. @ top reference is 0 dB.
Bottom trace: Input return loss response:
Vertical scale: 10 dB/Div. @ center reference is 0 dB
Horizontal scale for both traces: 60 MHz /Div.
Left edge is 7.7 GHz, right edge is 8.3 GHz

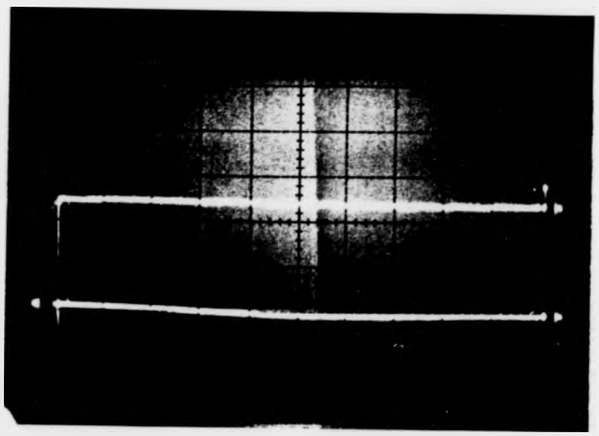


Figure 5.7.1.4 Amplitude and input return loss response between arm 1 and arm 4.

Top Trace : Amplitude response:
Vertical scale: 1 dB/ Div. @ top reference is 0 dB.
Bottom trace: Input return loss response:
Vertical scale: 10 dB/ Div. @ center reference is 0 dB
Horizontal scale for both traces: 60 MHz / Div.
Left edge is 7.7 GHz, right edge is 8.3 GHz.

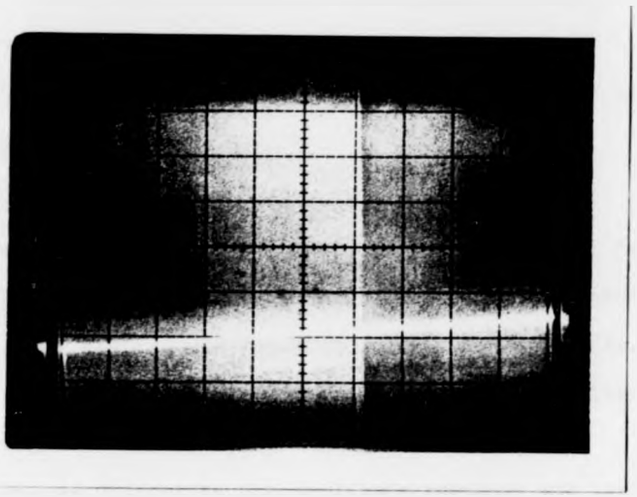


Figure 5.7.1.5. Isolation between arm 1 and arm 2.

Vertical scale: 10 dB/Div. @ center reference is 0 dB.

Horizontal scale : 60 MHz /Div.

Left edge is 7.7 GHz, right edge is 8.3 GHz.

From Figures 5.7.1.3 and 5.7.1.4, it is noted that the 3-dB coupler from arm 1 to arm 3 is -3.0 dB, while from arm 1 to arm 4 is -3.6 dB. The input return loss is 20 dB.

Figure 5.7.1.5 shows that the isolation between arm 1 and arm 2 is minimum 16 dB.

5.7.2 The performance of module 5

Figure 5.7.2.1 is the physical configuration of module 5. Figure 5.7.2.2 and Figure 5.7.2.3 show the amplitude response of the individual power devices FLM7785-8C(No.1) and FLM7785-8C(No.2) respectively, they were tested separately with special test fixture before being installed in the housing of the module 5.

Figure 5.7.2.4 is the amplitude response and input return loss of the balanced amplifier of module 5 with FLM7785-8C(No.1) and FLM7785-8C(No.2) installed. It is interesting to noted that the total circuit loss is only 0.8 dB over the 2.8 inch length of module 5, including four DC block capacitors and two 40 dB couplers for sampling the RF signal.

Table 5.7.2.1 is the delta-gain and delta-phase measurement results.

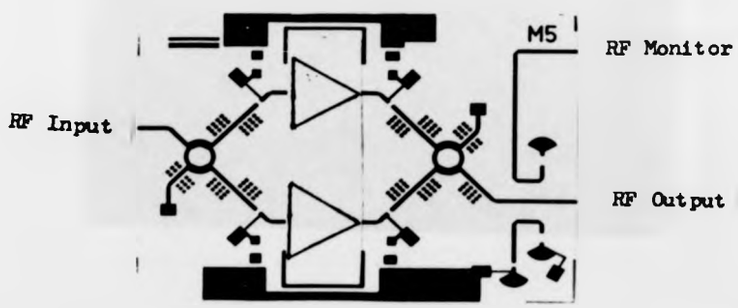


Figure 5.7.2.1 Configuration of module 5

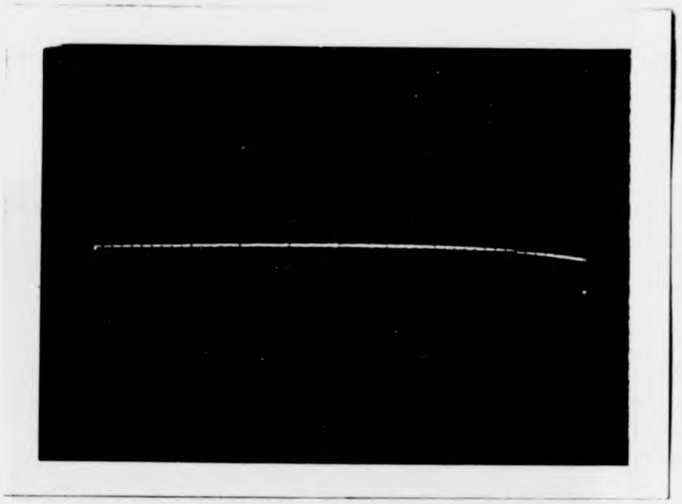


Figure 5.7.2.2 Amplitude response of single device FLM7785-8c no.1
Vertical scale: 1 dB/Div. Reference @ center line is 7.2 dB.
Horizontal scale: 60 MHz/Div. form 7.7 to 8.3 GHz.

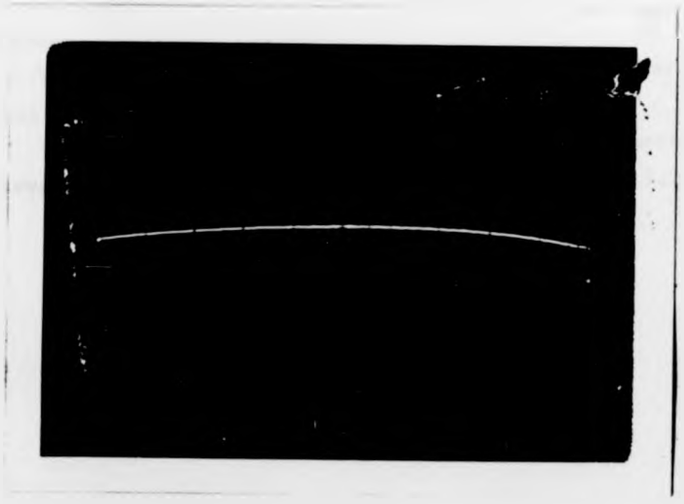


Figure 5.7.2.3 Amplitude response of single device FLM7785-8c no.2
Vertical scale: 1 dB/Div. Referance @ 7.4 dB of center line.
Horizontal scale: the same as Figure5.7.2.2.

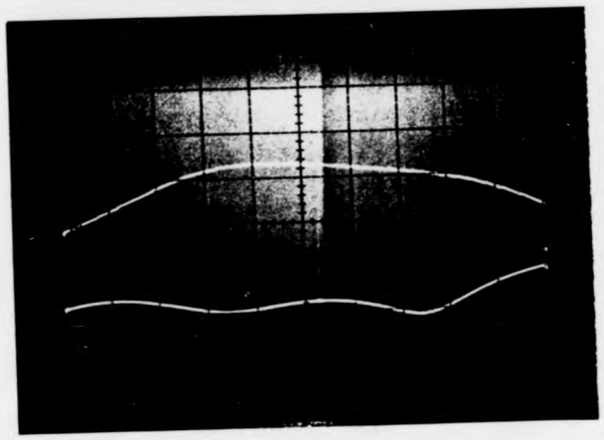


Figure 5.7.2.4 The amplitude and input return loss response of Module5

Top trace: Amplitude response:

Vertical scale: 1 dB/Div. at 6.4 dB at center line.

Bottom trace: Input return loss response:

Vertical scale: 10 dB/Div. reference line at center is 0 dB.

Horizontal scale for both traces : 60 MHz/Div. form 7.7 to 8.3 GHz

Table 5.7.2.1 The delta-gain and delta-phase measurement results of Module 5

MOD5 13:02:40

FREQ (GHz) = 7.7 GAIN (dBm) = 6.18

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)
27.00	33.18	0.00	0.00	-500.00	-1215.00	-1818.00	9.46
28.00	34.16	-.02	-.24	-500.00	-1215.00	-1822.00	9.46
29.00	35.12	-.06	-.06	-520.00	-1210.00	-1826.00	9.45
30.00	36.05	-.13	.06	-525.00	-1210.00	-1830.00	9.45
31.00	36.98	-.20	.38	-545.00	-1205.00	-1840.00	9.44
32.00	37.89	-.29	.80	-550.00	-1196.00	-1850.00	9.42
33.00	38.71	-.47	1.04	-575.00	-1190.00	-1870.00	9.40
34.00	39.44	-.74	1.38	-620.00	-1180.00	-1900.00	9.38
35.00	40.04	-1.14	1.78	-645.00	-1175.00	-1966.00	9.37
36.00	40.64	-1.54	2.24	-670.00	-1170.00	-2060.00	9.38
37.00	41.17	-2.01	2.30	-720.00	-1157.00	-2168.00	9.37

FREQ (GHz) = 8 GAIN (dBm) = 7.99

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)
27.00	34.99	0.00	0.00	-525.00	-1210.00	-1874.00	9.46
28.00	35.95	-.04	-.10	-550.00	-1205.00	-1904.00	9.45
29.00	36.89	-.10	.04	-575.00	-1199.00	-1954.00	9.44
30.00	37.69	-.30	.16	-625.00	-1189.00	-2010.00	9.44
31.00	38.43	-.56	.10	-705.00	-1171.00	-2060.00	9.42
32.00	39.08	-.91	.04	-815.00	-1148.00	-2108.00	9.41
33.00	39.69	-1.30	-.20	-1000.00	-1107.00	-2174.00	9.40
34.00	40.23	-1.76	-.68	-1200.00	-1066.00	-2228.00	9.38
35.00	40.63	-2.36	-.44	-820.00	-1142.00	-2092.00	9.39
36.00	41.02	-2.97	-.62	-355.00	-1231.00	-1970.00	9.39
37.00	41.35	-3.64	-1.10	25.00	-1300.00	-1916.00	9.38

FREQ (GHz) = 8.3 GAIN (dBm) = 7.33

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)	Igs (ua)	Vgs (mv)	Ids (ma)	Vds (V)
27.00	34.33	0.00	0.00	-525.00	-1213.00	-1830.00	9.46
28.00	35.32	-.01	-.14	-525.00	-1210.00	-1838.00	9.45
29.00	36.28	-.05	.02	-525.00	-1210.00	-1850.00	9.45
30.00	37.27	-.06	.32	-550.00	-1205.00	-1868.00	9.44
31.00	38.20	-.13	.62	-570.00	-1199.00	-1898.00	9.43
32.00	39.09	-.24	.66	-600.00	-1190.00	-1948.00	9.42
33.00	39.89	-.44	.38	-650.00	-1176.00	-2008.00	9.40
34.00	40.55	-.78	-.56	-735.00	-1156.00	-2078.00	9.38
35.00	41.02	-1.31	-1.90	-870.00	-1129.00	-2164.00	9.37
36.00	41.35	-1.98	-2.74	-1065.00	-1092.00	-2288.00	9.37
37.00	41.60	-2.73	-2.04	-585.00	-1185.00	-2224.00	9.38

5.7.3 ALC Circuit

The ALC is a feedback loop that samples the RF signal via 40 dB coupler and adjusts the DC bias current for the Module 2 PIN diode attenuation thus maintaining the output power at a constant level. A square law detector diode in the amplifier output module produces a voltage which is proportional to the RF output power. This voltage, through a control circuit as shown in Figure 5.7.3.1, is fed back to the PIN attenuator. thus if the output power tends to change, the attenuator bias current is adjusted to counteract that change. In order to minimize the range requirement of the ALC circuit, an open loop temperature compensation circuit is provided by a negative temperature coefficient thermistor which counteracts the gain changes associated with thermal characteristics of the transistors.

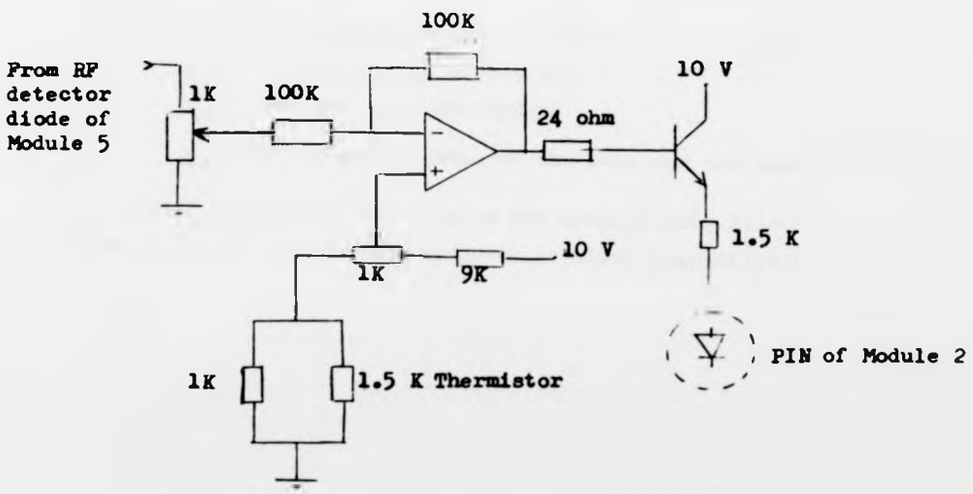


Figure 5.7.3.1 ALC configuration.

5.7.4 40 dB coupler

Microstrip coupler was built up by two edge-coupled microstrip lines with the electric length $L = \lambda_m / 4$ at the midband frequency(14)-(16). The coupling value C in dB is given as

$$C\ (\text{dB}) = 20 \log \left(\frac{1}{K}\right) \qquad (5.7.4.1)$$

where K is the coupling factor.

The even and odd mode line impedances are:

$$Z_{oe} = Z_o \frac{1 + K}{1 - K} \qquad (5.7.4.2)$$

$$Z_{oo} = Z_o^2 / Z_{oe} \qquad (5.7.4.3)$$

$$\lambda_m = \sqrt{\lambda_{oe}\ \lambda_{oo}} \qquad (5.7.4.4)$$

$$L = \lambda_m / 4 \qquad (5.7.4.5)$$

where Z_o : the characteristic impedance of the system

λ_{oe}: the even mode wavelength

λ_{oo}: the odd mode wavelength

λ_m : the geometric mean of the even and odd mode wavelemgths

Table 5.7.4.1 and Table 5.7.4.2 show the Compact data file of optimization of 40 dB coupler and analysis results, respectively.

```
CPL AA MS 24 -136.957 137 10.2 25
RES BB SE 50
CON AA T4 1 2 3 4
CON BB T2 3 0
CON BB T2 4 0
DEF CC T2 1 2
PRI CC S1 50
END
7000 9000 500
END
.001
0 0 1 -40
END
```

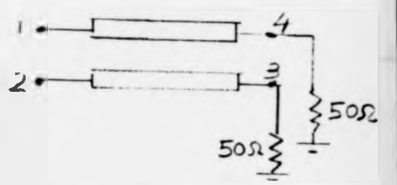


Table 5.7.4.1 COMPACT data file for optimization of 40 dB coupler

POLAR S-PARAMETERS IN 50.0 OHM SYSTEM

FREQ.	S11 (MAGN<ANGL)	S21 (MAGN<ANGL)	S12 (MAGN<ANGL)	S22 (MAGN<ANGL)	S21 DB
7000.00	.01< 10	.01< 10.3	.010< 10.3	.01< 10	-40.05
7500.00	.01< 5	.01< 4.7	.010< 4.6	.01< 5	-39.94
8000.00	.01< -1	.01< -1.0	.010< -1.0	.01< -1	-39.91
8500.00	.01< -7	.01< -6.7	.010< -6.7	.01< -7	-39.97
9000.00	.01< -12	.01< -12.4	.010< -12.4	.01< -12	-40.12

Table 5.7.4.2 COMPACT analysis results of 40 dB coupler

5.8 The performance of a complete amplifier

5.8.1 Frequency response

The amplifier was evaluted over a wide ambient temperature range from -10°C to 50°C under forced air cooling condition. Figure 5.8.1 shows the output power versus frequency at three temperatures, -10°C, 27°C and 50°C.

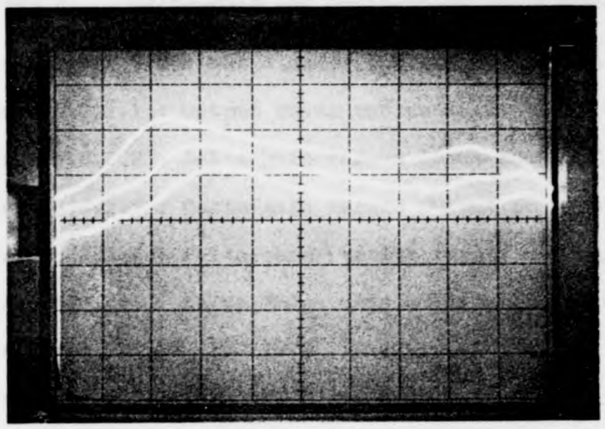


Figure 5.8.1 Output power versus frequency:
Top trace : At -10°C
Center trace : At 27°C
Bottom trace : At 50°C
Vertical scale: 1dB/Div. Center line is calibrated to 40 dBm
Horizontal scale : 60 MHz/Div., from 7.7 to 8.3 GHz

The variation in output power over the temperature range was 1.8 dB maximum at rated output power.

5.8.2 Output Power versus Input Power and AM/AM and AM/PM conversion Characteristics

Using automatic measurement technique developed in Chapter 2, a P_{in} versus P_{out}, delta-gain and delta-phase measurement results are shown in Tabel 5.8.2 and Figures 5.8.2.1 to 5.8.2.5.

Figure 5.8.2.1 : Output Power versus Input power of the SSPA

Figure 5.8.2.2 : Delta-gain versus Input power of the SSPA

Figure 5.8.2.3 : Delta-gain versus Output power of the SSPA

Figure 5.8.2.4 : Delta-phase versus Input power of the SSPA

Figure 5.8.2.5 : Delta-Phase versus Output power of the SSPA

Photograph 5.8.1 : Module 1

Photograph 5.8.2 : Module 2 and Module 3

Photograph 5.8.3 : Module 4

Photograph 5.8.4 : Module 5

Photograph 5.8.5 : The Prototype 8 GHz,10 W SSPA with the housing cover removed.

At 40 dBm output power level with ALC circuit in the "OFF" position, the corresponding input power level is -12 dBm at 8 GHz, the AM/AM conversion factor, defined as Δ Pout/ΔPin, is calculated from the slope at -12 dBm,

$$\frac{1.23-0.48}{2} = 0.375 \text{ dB/dB}$$

The AM/PM conversion factor, defined as Δ Phase /Δ Pin, is calculated from the slope at -12 dBm in Figure5.8.2.4,i.e.

$$\frac{3.98-2.30}{2} = 0.84^{\circ}/\text{dB}$$

Table 5.6.2 The measurement results of the 8-GHz, 10 watt SSPA

FREQ (GHz) = 7.7 GAIN (dBm) = 50.82

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
-15.00	35.82	0.00	0.00
-14.00	36.69	-.13	.66
-13.00	37.55	-.27	1.74
-12.00	38.37	-.45	2.46
-11.00	39.05	-.77	2.72
-10.00	39.76	-1.06	2.50
-9.00	40.29	-1.53	2.40
-8.00	40.72	-2.10	2.40
-7.00	41.06	-2.76	2.48
-6.00	41.28	-3.54	2.16
-5.00	41.45	-4.37	1.32
-4.00	41.49	-5.33	1.16
-3.00	41.61	-6.21	.12
-2.00	41.65	-7.17	-.62

FREQ (GHz) = 8 GAIN (dBm) = 52.79

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
-15.00	37.79	0.00	0.00
-14.00	38.58	-.21	.96
-13.00	39.31	-.48	2.30
-12.00	39.97	-.82	3.34
-11.00	40.56	-1.23	3.98
-10.00	41.05	-1.74	5.50
-9.00	41.49	-2.30	6.72
-8.00	41.79	-3.00	7.92
-7.00	42.01	-3.78	10.68
-6.00	42.15	-4.64	14.00
-5.00	42.26	-5.53	17.52
-4.00	42.34	-6.45	21.24
-3.00	42.45	-7.34	24.20
-2.00	42.64	-8.15	26.62

FREQ (GHz) = 8.3 GAIN (dBm) = 52.56

INPUT (dBm)	OUTPUT (dBm)	Del-Gain (dB)	Del-Phase (dgrees)
-15.00	37.56	0.00	0.00
-14.00	38.44	-.12	.18
-13.00	39.22	-.34	-.22
-12.00	39.85	-.71	-1.40
-11.00	40.30	-1.26	-2.74
-10.00	40.63	-1.93	-4.14
-9.00	40.93	-2.63	-5.26
-8.00	41.14	-3.42	-6.06
-7.00	41.35	-4.21	-6.38
-6.00	41.58	-4.98	-5.20
-5.00	41.74	-5.82	-2.70
-4.00	41.84	-6.72	-.16
-3.00	41.91	-7.65	2.16
-2.00	42.03	-8.53	4.08

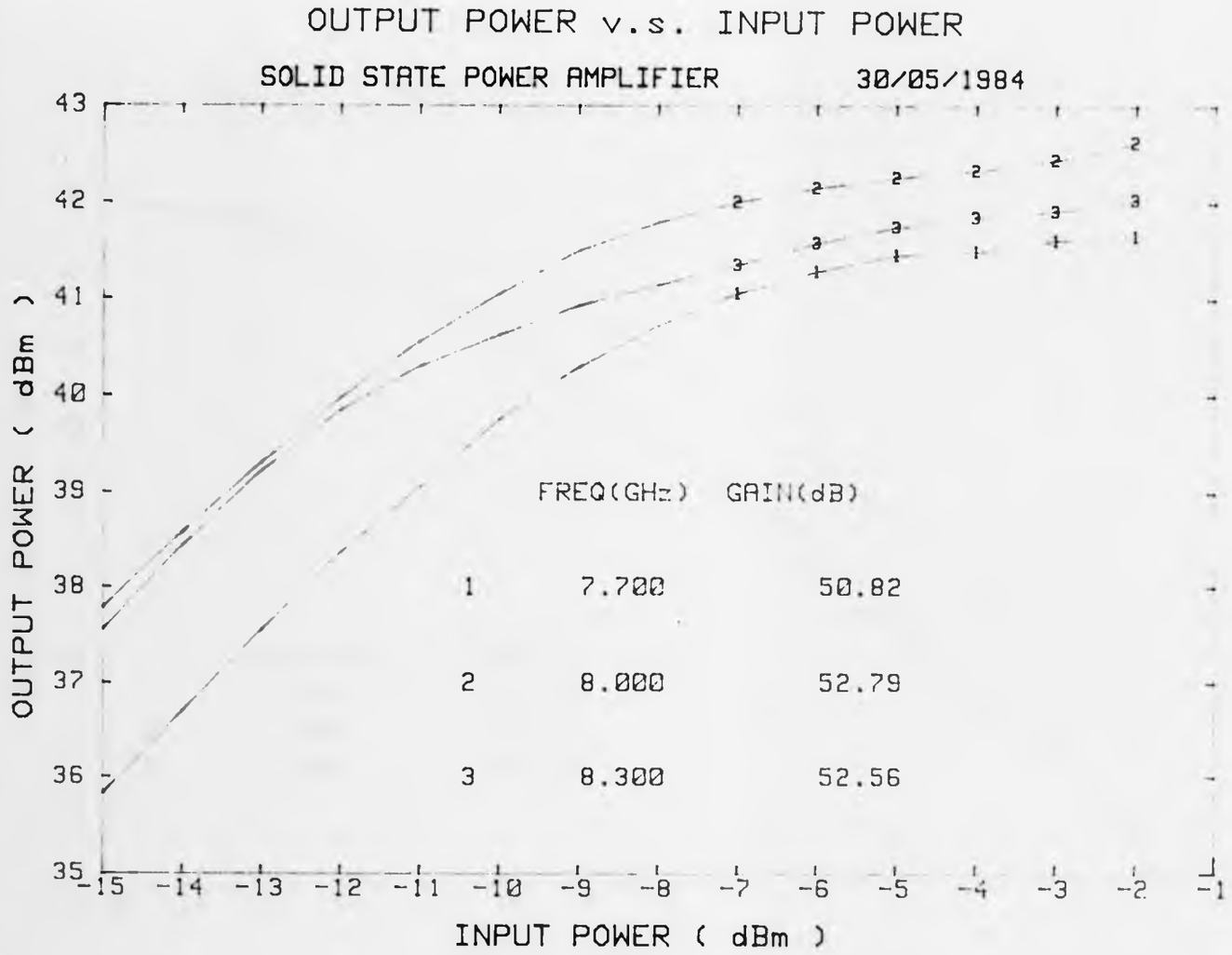


Figure 5.8.2.1 Output Power versus Input Power of the SSPA

Figure 5.8.2.2 Delta-Gain versus Input Power of the SSPA

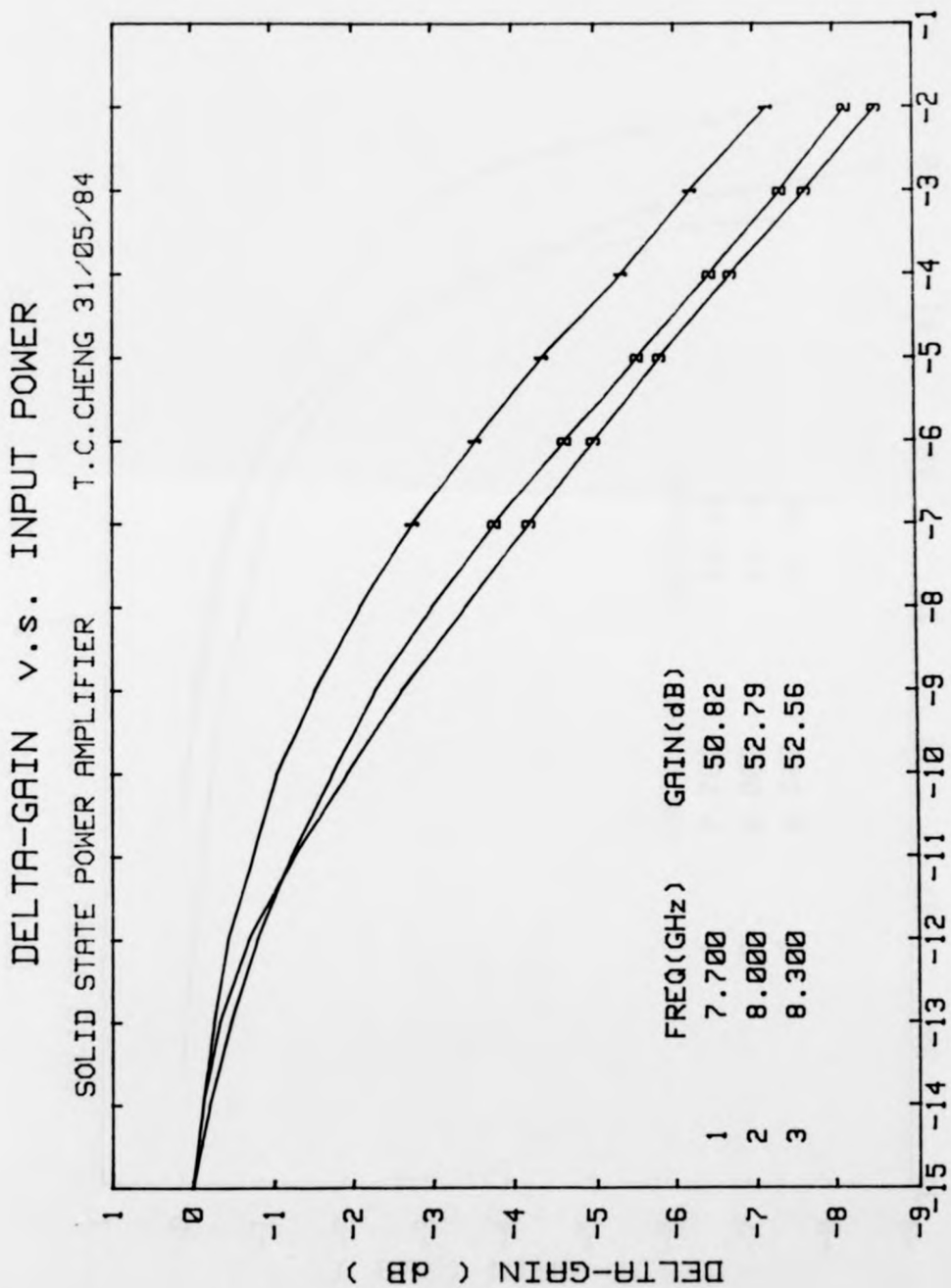


Figure 5.8.2.3 Delta-Gain versus Output Power of the SSPA

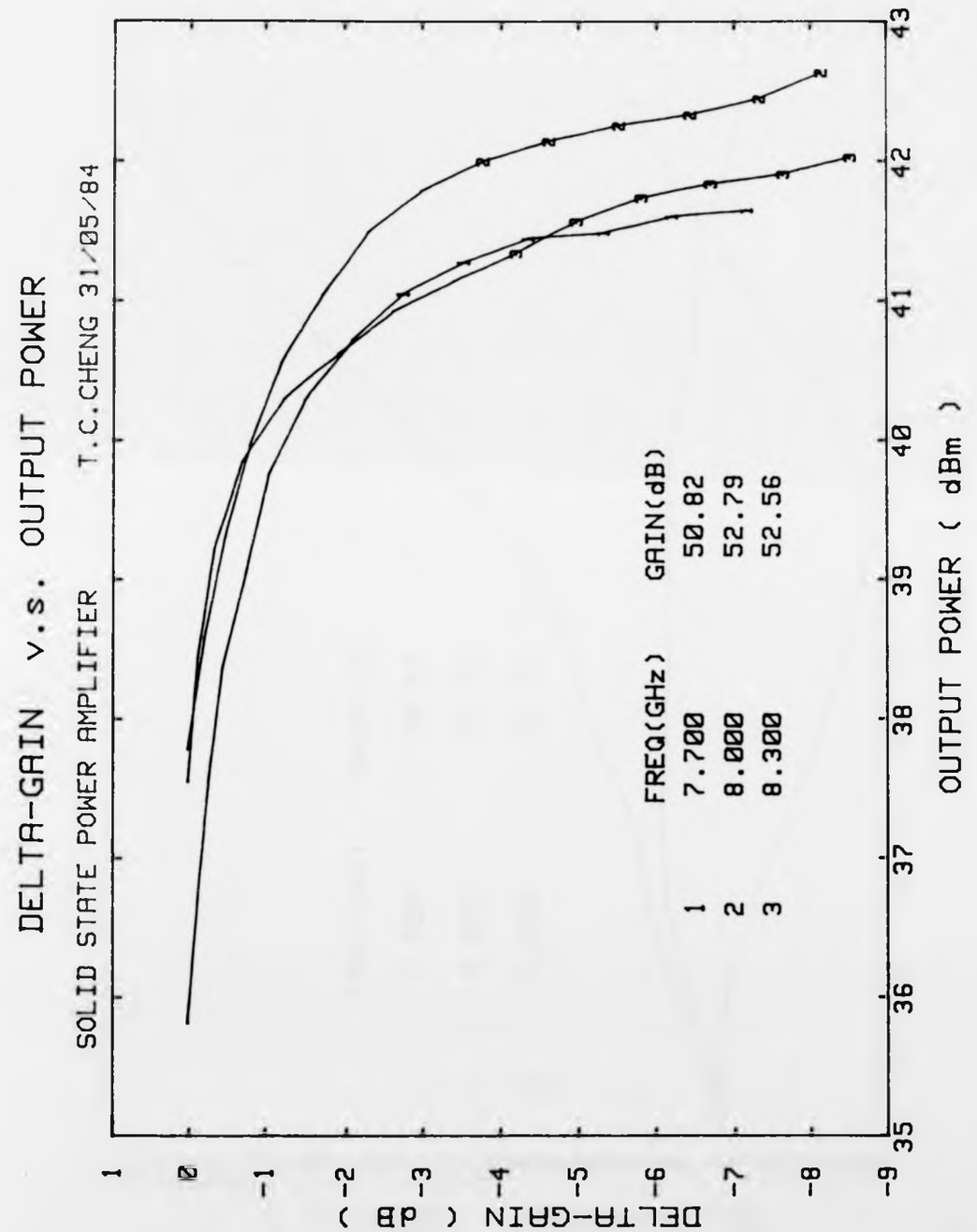


Figure 5.8.2.4 Delta-Phase versus Input Power of the SSPA

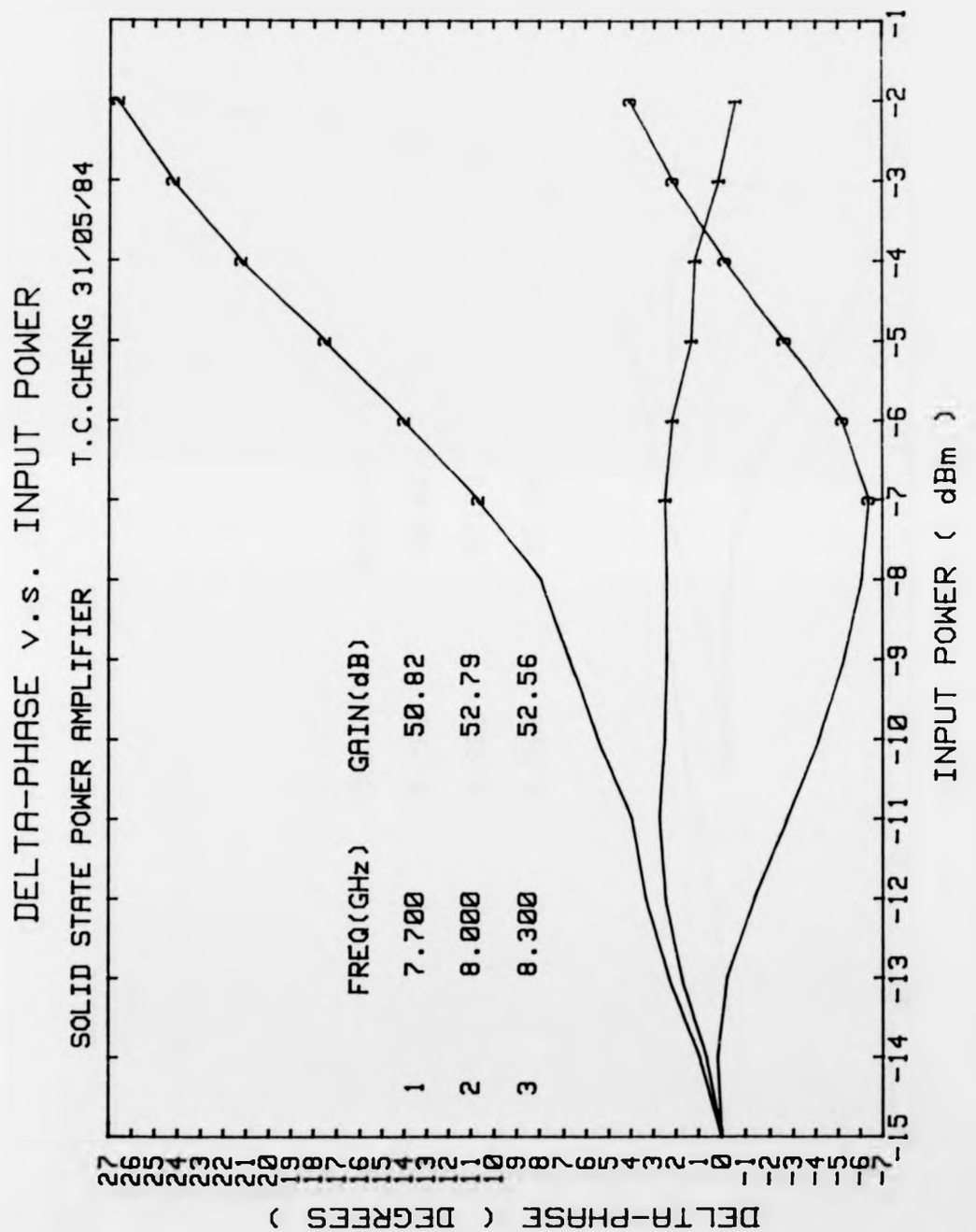
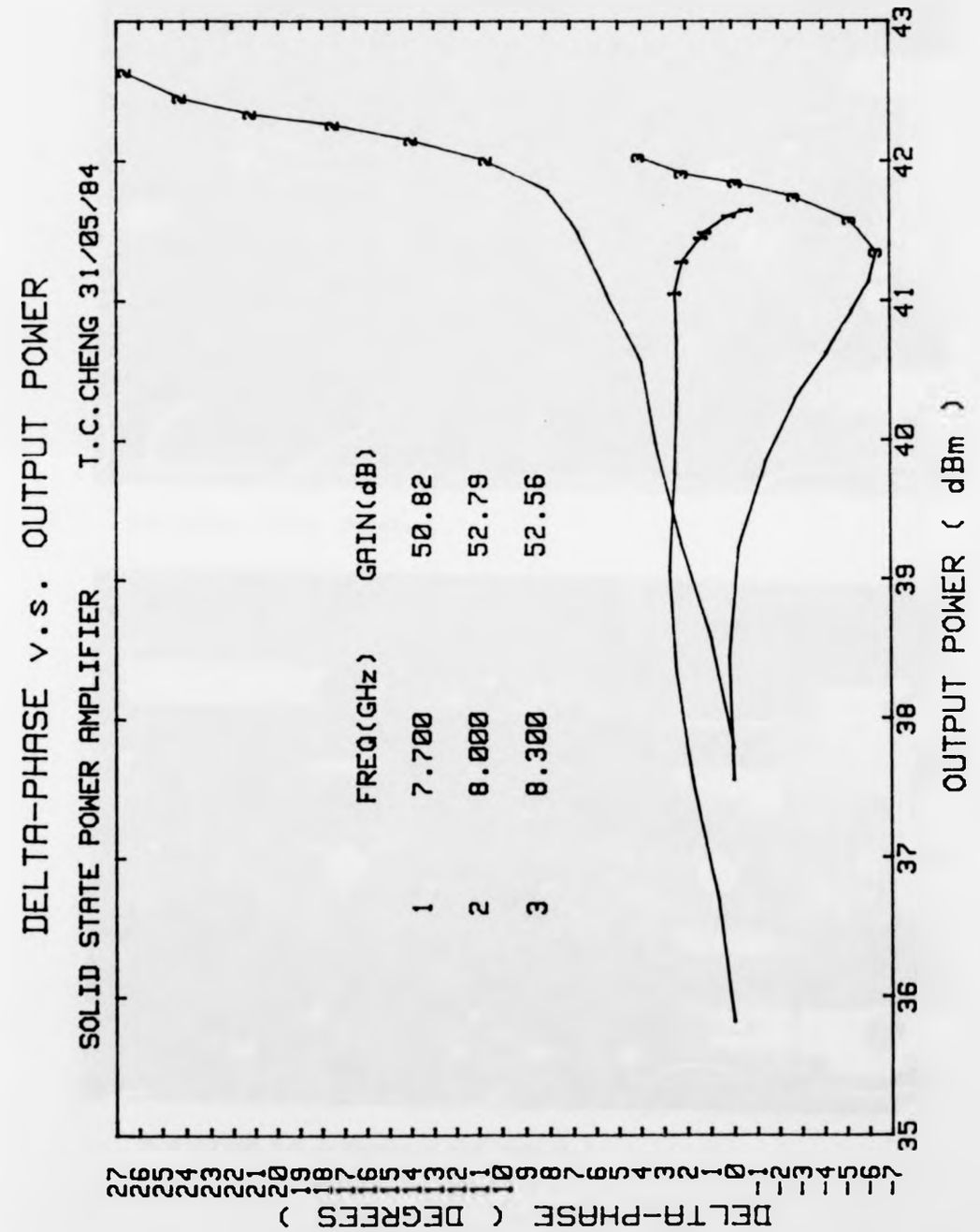
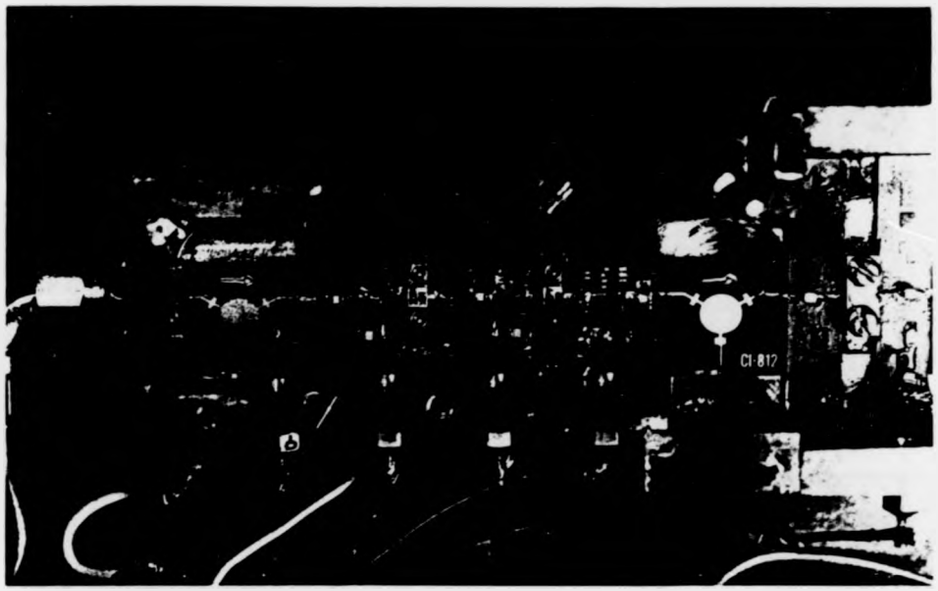
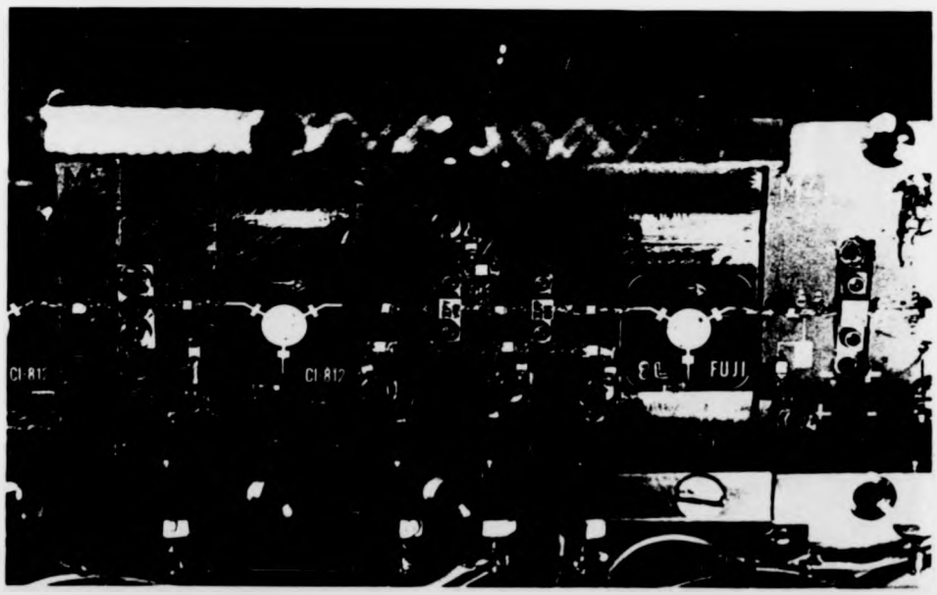


Figure 5.8.2.5 Delta-Phase versus Output Power of the SSPA

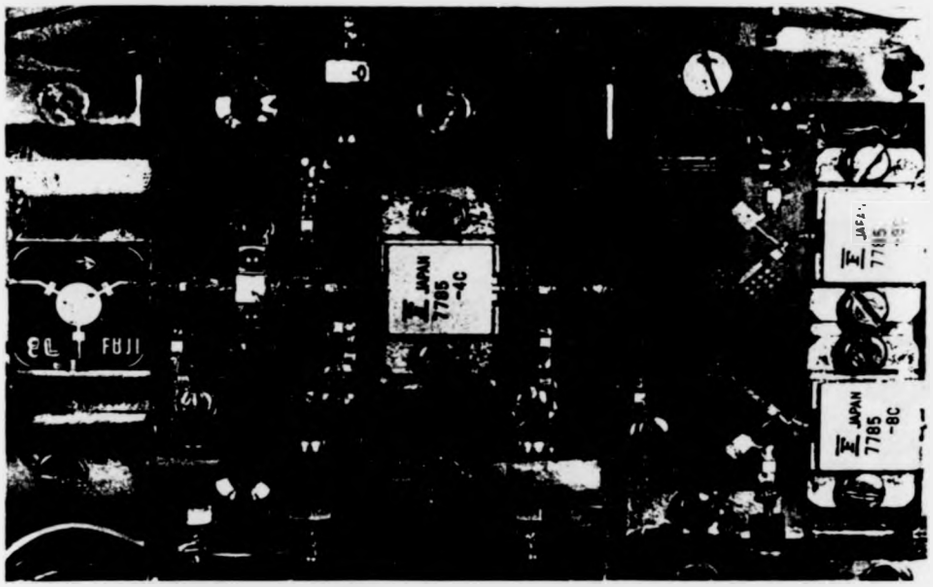




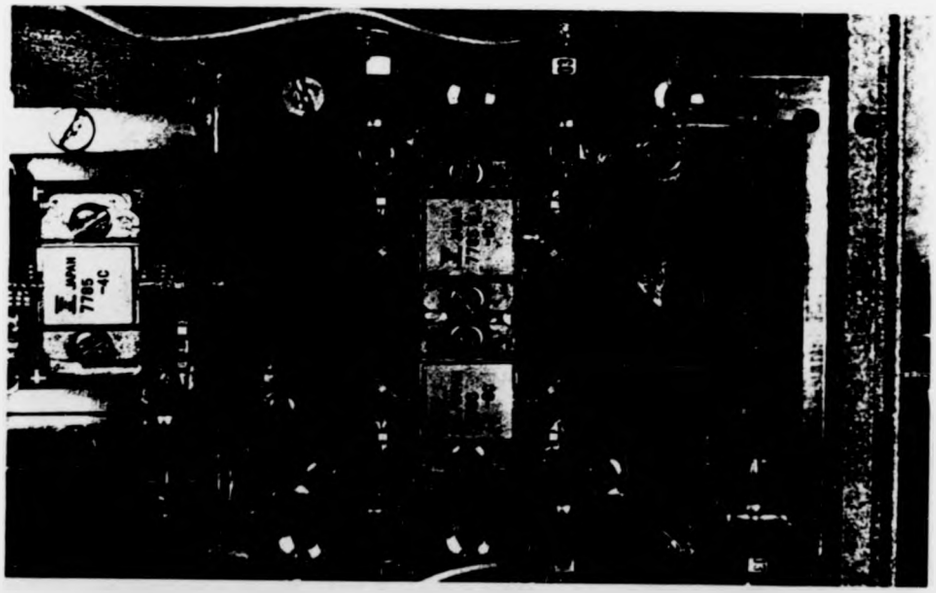
Photograph 5.8.1 Module 1



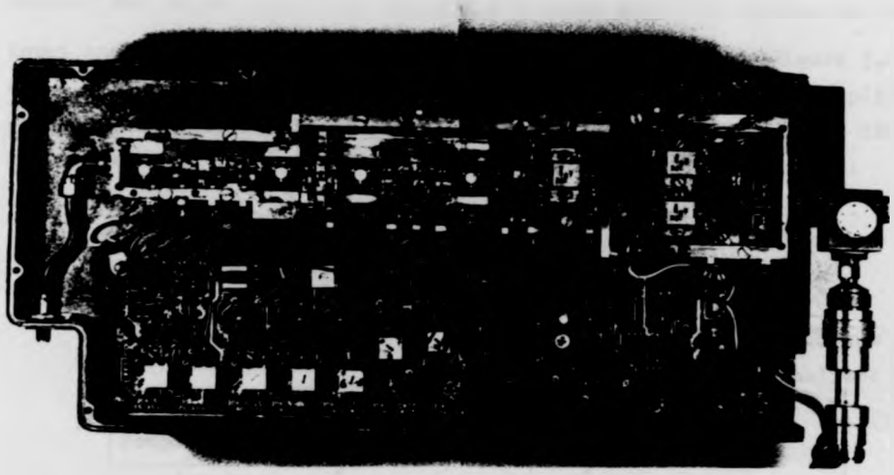
Photograph 5.8.2 Module 2 and Module 3



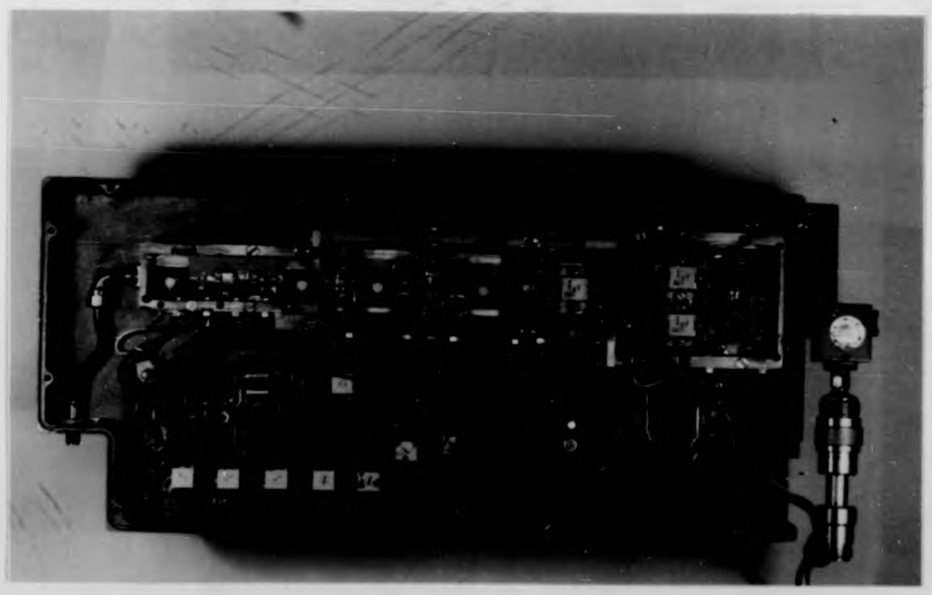
Photograph 5.8.3 Module 4

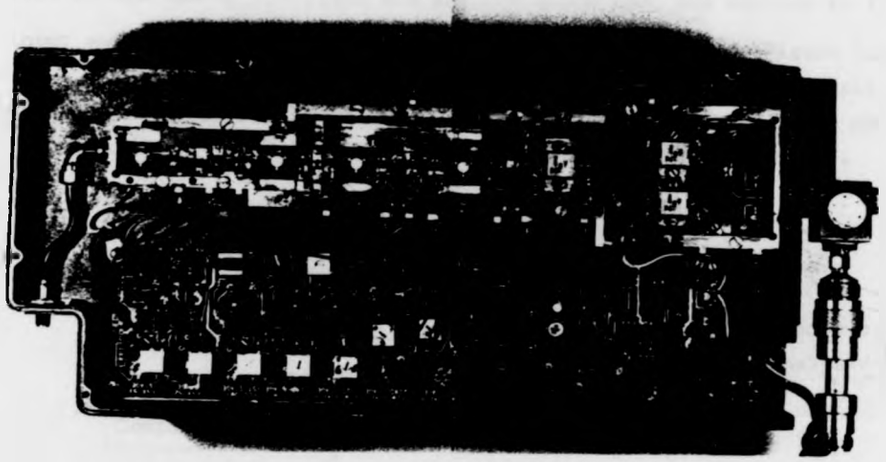


Photograph 5.8.4 Module 5

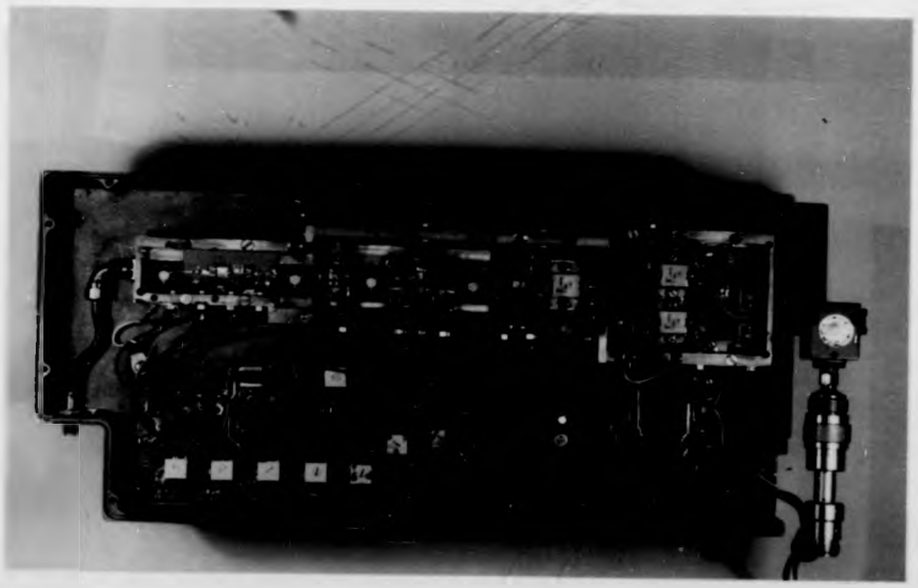


Photograph 5.8.5 8-GHz 10 Watt Solid State Power Amplifier





Photograph 5.8.5 8-GHz 10 Watt Solid State Power Amplifier



5.8.3 Third-Order Intermodulation Distortion

Third-order intermodulation distortion IMD_3 of the amplifier is measured using the method described by Heiter(17). Two single frequencies with 10 MHz apart, f_1= 7.990 GHz and f_2= 8.000 GHz, are applied to the input and the amplifier output is observed on an analyser. Figure 5.8.1 shows a typical measurement set up. Frequency spectrums of the amplifier with output power levels: 37.18,38.07,38.70,39.30,39.79 and 40.22 dBm at frequency of 7.990 GHz are shown in Figures 5.8.3.2 to 5.8.3.7.

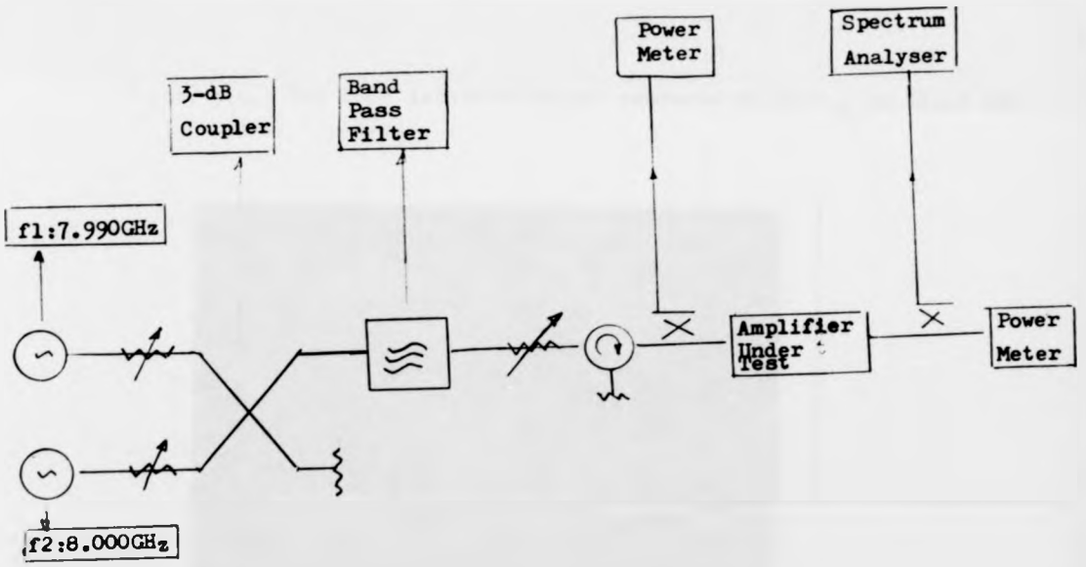


Figure 5.8.1 Third-Order Intermodulation Distortion

Two Tone Measurement Set Up.

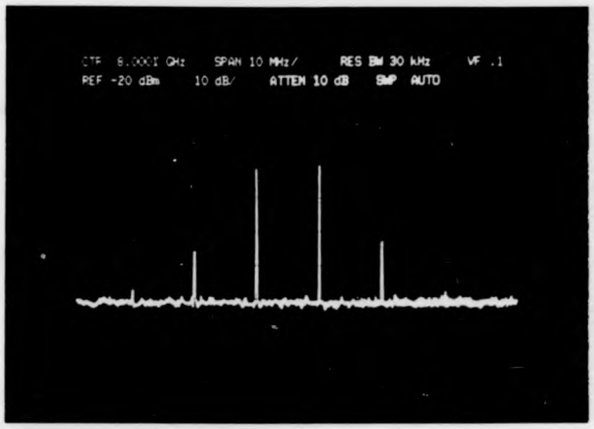


Figure 5.8.2 Two tone intermodulation products at $P_{out(f_1)}$ = 37.18 dBm

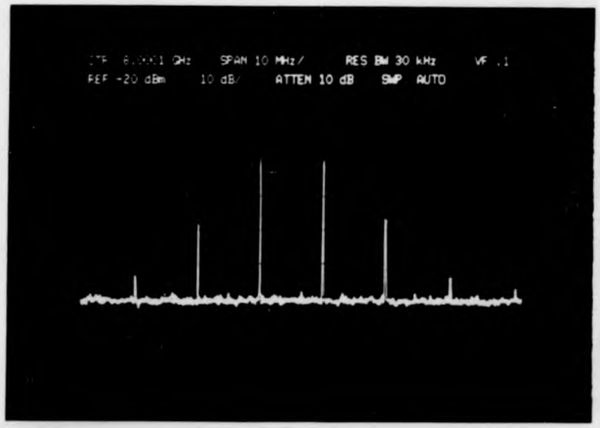


Figure 5.8.3 Two tone intermodulation products at $P_{out(f_1)}$ = 38.07 dBm

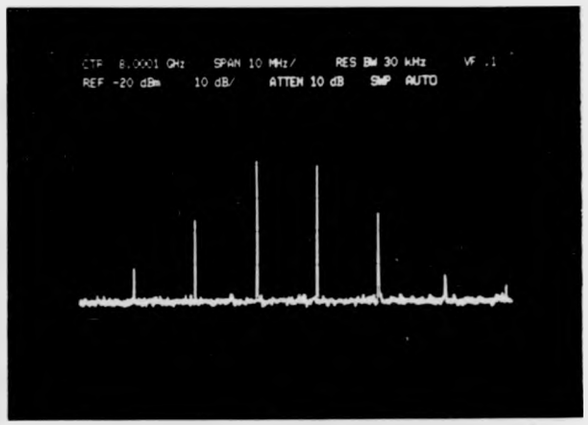


Figure 5.8.4 Two tone intermodulation products at $Pout_{(f_1)} = 38.70$ dBm

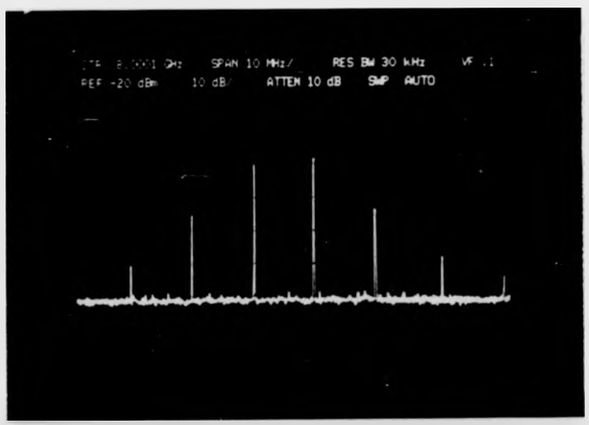


Figure 5.8.5 Two tone intermodulation products at $Pout_{(f_1)} = 39.30$ dBm

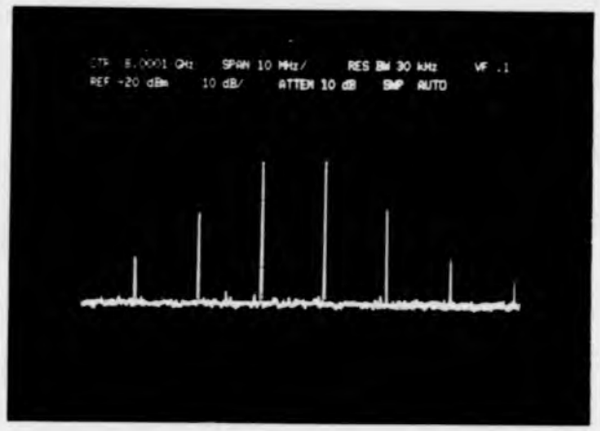


Figure 5.8.6 Two tone intermodulation products at $Pout_{(f_1)}$ = 39.79 dBm

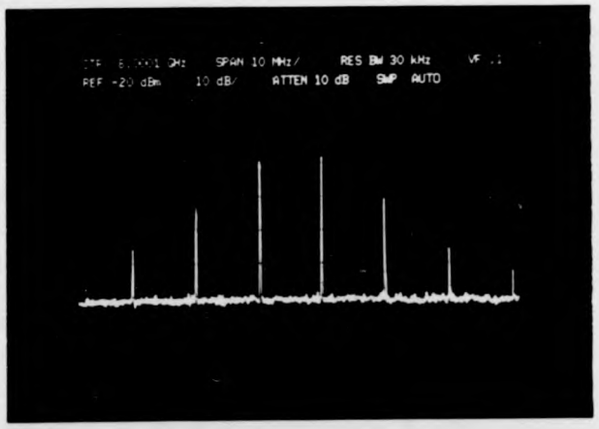


Figure 5.8.7 Two tone intermodulation products at $Pout_{(f_1)}$ = 40.22 dBm

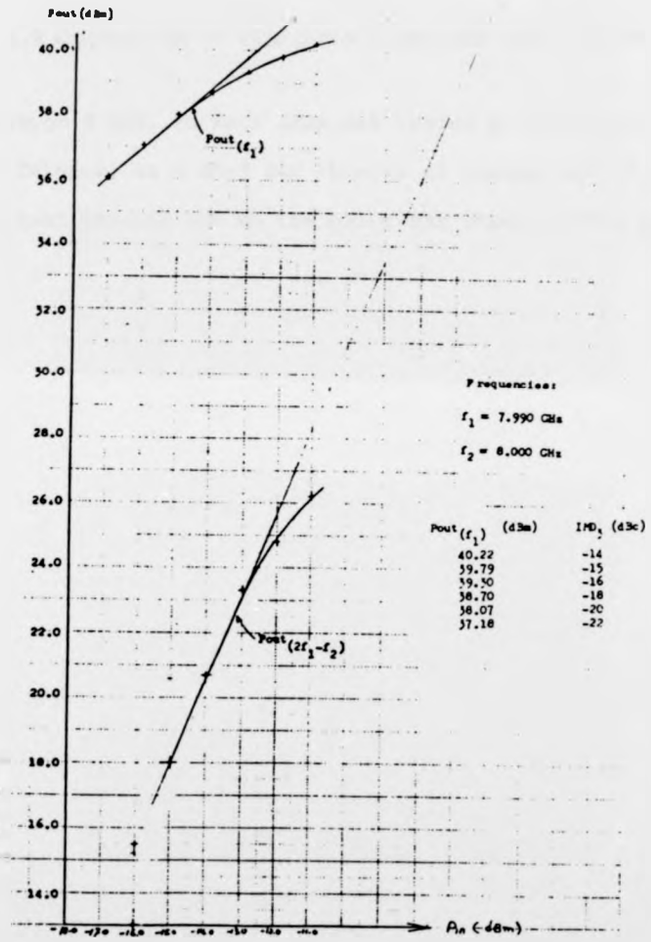


Figure 5.8.3.8 The third order intermodulation intercept point

The ratio of the two (equal) carrier levels to the level of the third order intermodulation products is expressed in dBc. The measurement results are shown in Figure 5.8.3.8. The extrapolated third order intermodulation intercept is 48.5 dBm.

5.9 COMPARISON OF PERFORMANCE BETWEEN SSPA AND TWTA

The Prototype 8 GHz, 10 Watt SSPA was tested by Alleyne(18) of Northern Telecom, in a RD-3 Bay line-up at channel A4' (f_c= 8173.15 MHz).

The test results are on the following pages of this Section.

5.9.1 TRANSMITTER AMPLITUDE RESPONSE TEST

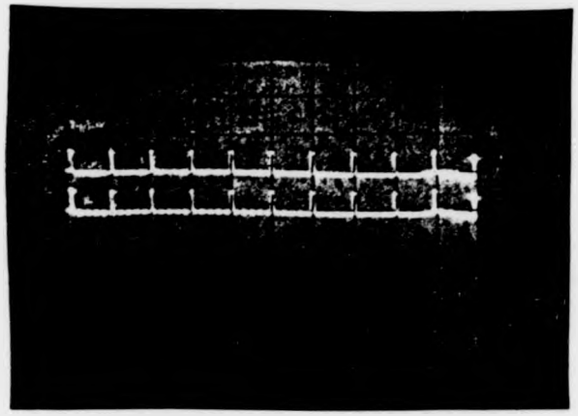


Figure 5.9.1.1 I.F. Amplitude Response for SSPA

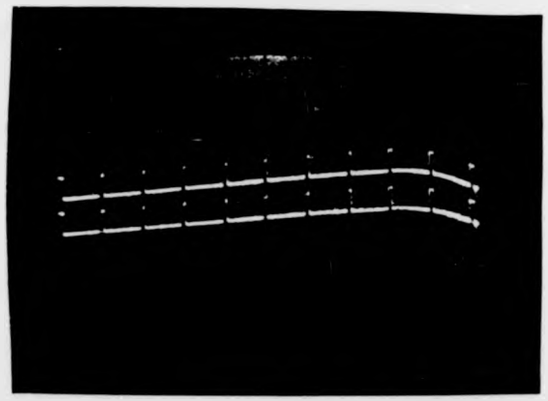
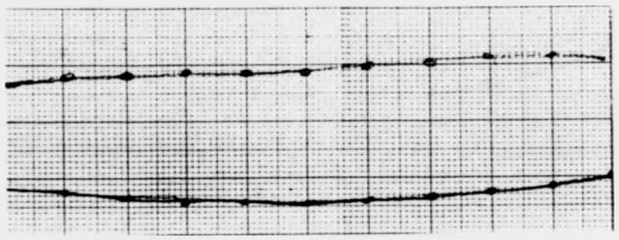


Figure 5.9.1.2 I.F. Amplitude Response for TWT

Vertical Scale: 0.7 dB / Div.

Horizontal Scale : The Peak to Peak Amplitude Ripple Between 115 and 165 MHz $\leq$ 0.4 dB

5.9.2 HOP I.F. TO I.F. AMPLITUDE RESPONSE AND GROUP DELAY TESTS AT 40 dBm OUTPUT POWER LEVEL



Top Curve: Amplitude Response

Vertical Scale : 1 dB / Div.

Horizontal Scale : 2.0 MHz / Div

(From 130 to 150 MHz)

Requirement : The Amplitude Slope Between 130 and 150 MHz $< \pm .5$ dB

The Amplitude Ripple $<$ 0. 1 dB Peak to Peak

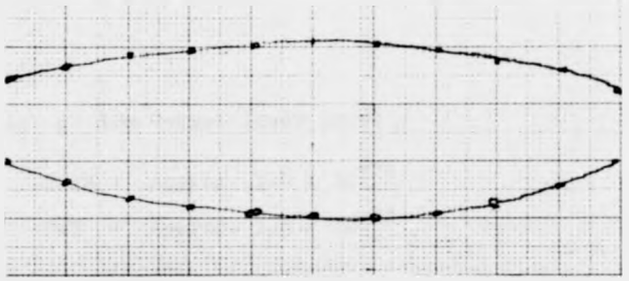
Bottom Curve: Group Delay

Vertical Scale : 10 ns / Div.

Horizontal Scale : Ditto

Requirement : The Group Delay Ripple Between 130 and 150 MHz $\leq$ 10 ns Peak to Peak

Figure 5.9.2.1 Hop I.F. to I.F Amplitude Response and Group Delay Response for SSPA.



Top Curve: Amplitude Response

Vertical Scale : 1 dB / Div.

Horizontal Scale : 2.0 MHz / Div

(From 130 to 150 MHz)

Requirement : The Amplitude Slope Between 130 and 150 MHz $< \pm .5$ dB

The Amplitude Ripple $<$ 0. 1 dB Peak to Peak

Bottom Curve: Group Delay

Vertical Scale : 10 ns / Div.

Horizontal Scale : Ditto

Requirement : The Group Delay Ripple Between 130 and 150 MHz $\leq$ 10 ns Peak to Peak

Figure 5.9.2.2 Hop I.F to I.F. Amplitude Response and Group Delay Response for TWT

5.9.3 RESIDUAL BIT ERROR RATE (BER)

At 40 dBm Output Power Level :

SSPA : Approx. 1.0×10^{-32}

TWT : Approx. 1.0×10^{-23}

At 42 dBm Output Power Level : (SSPA Saturated at 42 dBm)

SSPA : Approx. 1.0×10^{-32}

TWT : Approx. 2.2×10^{-21}

At 37 dBm Output Power Level :

SSPA : 7×10^{-28}

TWT : 6×10^{-23}

Figure 5.9.3.1 and Figure 5.9.3.2 show residual BER for the Solid State P.A. (SSPA) and the TWT P.A. respectively.

5.9.3 RESIDUAL BIT ERROR RATE (BER)

At 40 dBm Output Power Level :

SSPA : Approx. 1.0×10^{-32}

TWT : Approx. 1.0×10^{-23}

At 42 dBm Output Power Level : (SSPA Saturated at 42 dBm)

SSPA : Approx. 1.0×10^{-32}

TWT : Approx. 2.2×10^{-21}

At 37 dBm Output Power Level :

SSPA : 7×10^{-28}

TWT : 6×10^{-23}

Figure 5.9.3.1 and Figure 5.9.3.2 show residual BER for the Solid State P.A. (SSPA) and the TWT P.A. respectively.

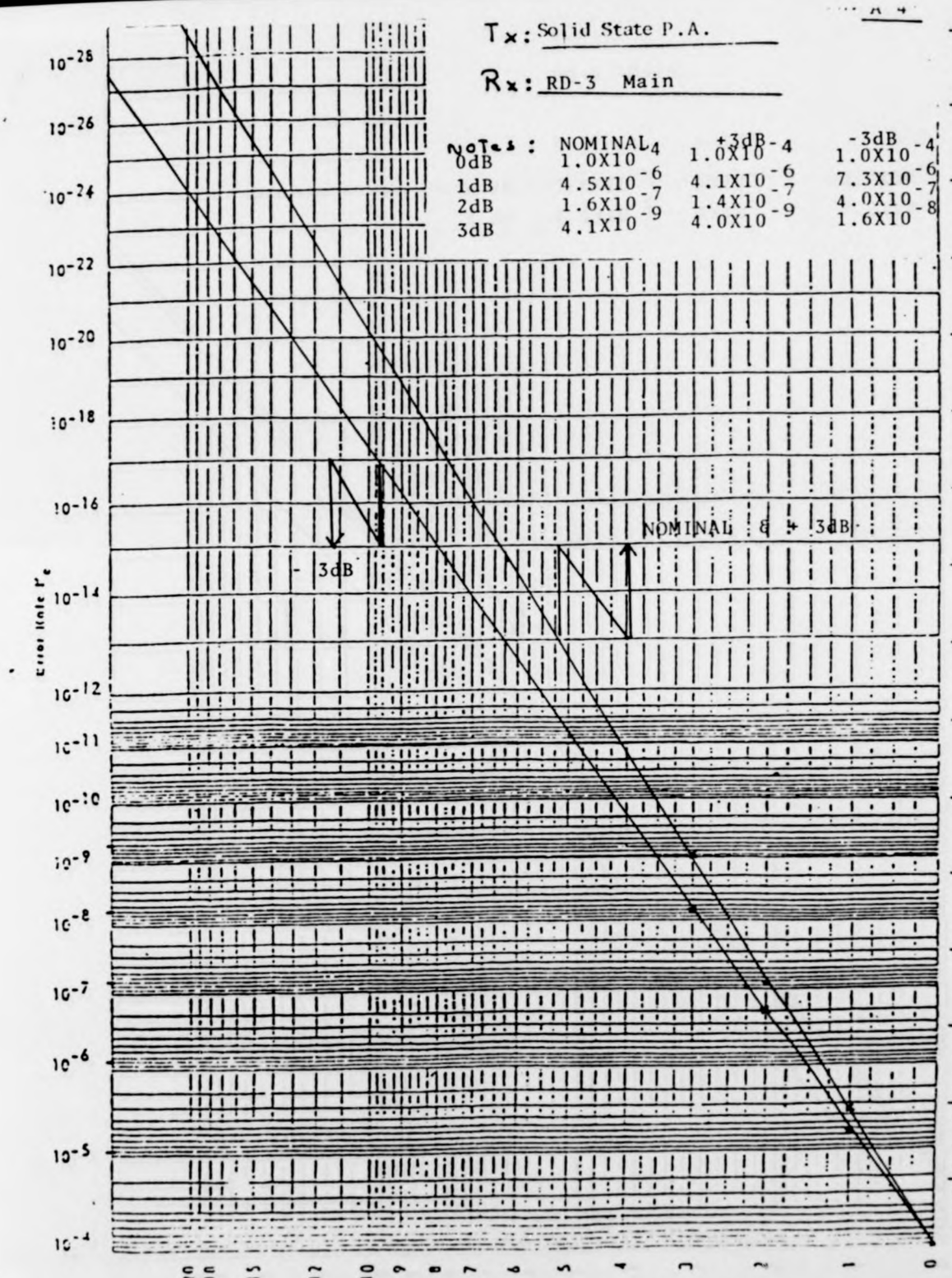

Tx: Solid State P.A.
Rx: RD-3 Main
NOTES:
NOMINAL
+3dB
-3dB
0dB 1.0X10-4 1.0X10-4 1.0X10-4
1dB 4.5X10-6 4.1X10-6 7.3X10-6
2dB 1.6X10-7 1.4X10-7 4.0X10-7
3dB 4.1X10-9 4.0X10-9 1.6X10-8
NOMINAL & + 3dB
- 3dB
Error Rate Pe
10-28
10-26
10-24
10-22
10-20
10-18
10-16
10-14
10-12
10-11
10-10
10-9
10-8
10-7
10-6
10-5
10-4
20
15
12
10
9
8
7
6
5
4
3
2
1
0
11.
10.
10.
9.5
9.0
8.5
8.0
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5

Figure 5.9.3.1

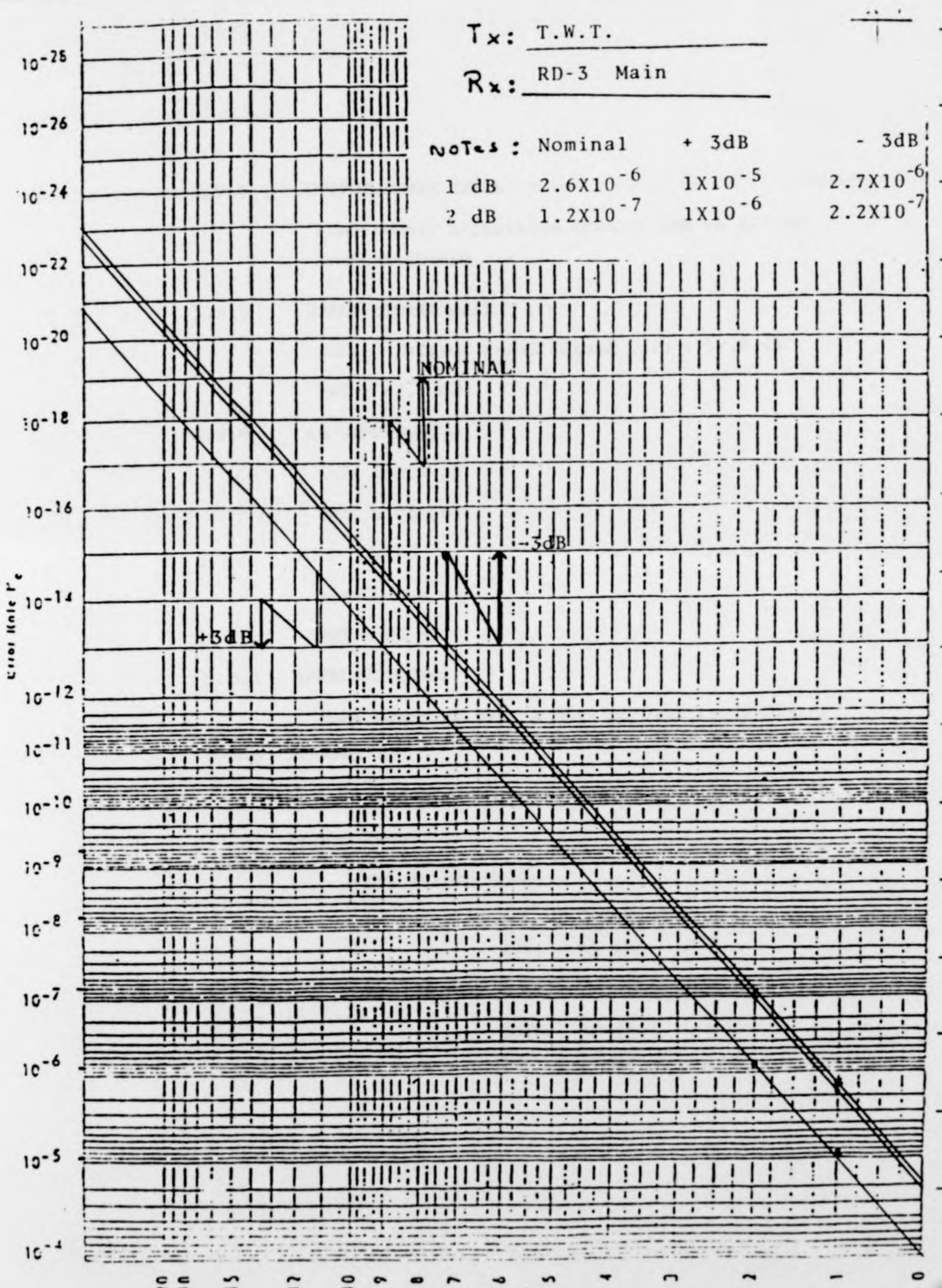

Tx: T.W.T.
Rx: RD-3 Main
NOTES : Nominal + 3dB - 3dB
1 dB 2.6X10^-6 1X10^-5 2.7X10^-6
2 dB 1.2X10^-7 1X10^-6 2.2X10^-7
NOMINAL
-3dB
+3dB
Error Rate Pe
10^-25
10^-26
10^-24
10^-22
10^-20
10^-18
10^-16
10^-14
10^-12
10^-11
10^-10
10^-9
10^-8
10^-7
10^-6
10^-5
10^-4
11.
10.
10.
9.5
9.0
8.5
8.0
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
20
15
12
10
9
8
7
6
5
4
3
2
1
0

Figure 5.9.3.2

5.9.4 OUTPUT POWER LEVEL

Continously adjustable from 22 dBm to 42 dBm nominal 40 dBm.

5.9.5 SMALL SIGNAL GAIN

SSPA: Maximum Small Signal Gain : 52.8 dB

TWT : 43.4 dB

5.9.6 AM COMPRESSION

SSPA : 2.2 dB

TWT : 26 dB

5.9.7 NOISE FIGURE

SSPA: 7.6 dB

TWT : 24 dB

5.9.8 SPURIOUS TONES

None observed over a band of 0.01 to 18 GHz

5.9.9 HARMONICS

Without LPF (low pass filter) : 36 dBc

5.7.10 RETURN LOSS:

Input Return Loss

SSPA: 20 dB

TWT : 15 dB

Output Return Loss

SSPA: 20 dB

TWT : 10 dB

5.9.11 D.C. POWER DISSIPATION

V.D.C. = 10.0V , I.D.C. = 6.5 Amps

Power dissipated = 65 watts

5.9.12 OUTPUT MONITOR LEVEL

For nominal output power + 1.3dBM

Comments: No attempt was made to perform the R.F. leakage test, since the prototype model was not properly sealed.

Conclusion: A careful analysis of the test results showed that the solid state P.A. out performed the T.W.T..P.A. This was clearly demonstrated in the residual BER test where one saw that at nominal output level, the BER for the Solid State P.A. was much better than that of the T.W.T. P.A. Further, for a 3dB increase in output level the solid state P.A. ; showed no degradation. Only for a 3dB decrease in output level did the T.W.T. P.A. BER showed no degradation. On the strength of the results that were obtained the solid state P.A. showed that it would be more than a suitable replacement for the T.W.T. P.A.

5.10 REFERENCES:

1. " RD-3 Digital Microwave Radio," Northern Telecom Practice, Section 415-3000-100, Issued 10th Oct., 1981, pp.1-28.
2. Anderson,C.W., and Barber,S.G.:" Modulation Considerations for a 91 Mbit/s Digital Radio," IEEE Trans., 1978,COM-26,No.5
3. Brehm,G.E. et al.:" Biasing FETs for Optimum Performance," Microwaves,February,1974,pp.38-44.
4. Vendelin,G.D.:" Five Basic Bias Designs for GaAs FET Amplifier," Microwaves, February, 1978,pp.40-42.
5. Hunton,J.K. et al.:" Microwave Variable Attenuators and Modulators Using PIN Diodes," IRE Transactions on Microwave Theory and Techniques, July 1962,pp. 262-273.
6. Horkin,R.R.:" An Improved PIN Diode Attenuator for High Reliability MIC Applications," 1982 IEEE MTT-S Digest,pp.422-424.
7. Kurokawa,K.:"Design theory of balanced transistor amplifiers," Bell Syst. Tech.J.,44,No.10,1965,pp.1675-1698.
8. Russell,K.J.:" Microwave Power Combining Techniques," IEEE Trans. Microwave Theory Tech.,MTT-27,No.5,1979,pp.472-478.
9. Wilkinson,Ernest J.:" An N-WAY HYBRID Power Divider," PGMTT Transactions,Jan.,1960,pp.116-118.
10. Wilkinson,E.J.,and Sommers,D.J.:" Variable multiport power combiners," Microwave J.,21,No.2,1978,pp.59-63.
11. Morse,A.W.:" Modify combiner design to team high power amps," Microwaves,17,No.1,1978,pp.70-79.
12. Reed,J. and Wheeler,G.J.:" A Method of Analysis of Symmetrical four Port Networks," IRE Transactions on Microwave Theory and Techniques,October 1956,pp.246-252.
13. Gottfired,B.S., and Weisman,J.:" Introduction to Optimization Theory," Prentice Hall, 1973.pp.80-84.

14. Beyant,T.,and Weiss,J.:" Parameters of Microstrip transmission Lines and of Coupled Pairs of Microstrip Lines," IEEE Trans., MTT-16,1968,pp.1021-1027.

15. Jone,E.M.T. et al :" Coupled-Strip-Transmission-Line Filters and Lirectional Couplers," IRE Trans.,MTT-4,1956.pp.75-81.

16. Schneider,M.V.:" Microstrip Lines for Microwave Integrated Circuits," The Bell System Tech. J. , May-June, 1969.pp.1421-1444.

17. Heiter,G.L.:" Characterization of Nonlinearity in Microwave Devices and System," IEEE Trans.,1973,MTT-21,pp.797-804.

18. Alleyne,G.,:" RD-3 Solid State Power Amplifier TEST ," Northern Telecom Memorandum DeptX441, May 28th 1984.

CHAPTER 6 THERMAL STUDY OF A HIGH POWER AMPLIFIER

Many solid state RF designs were done in the past with little concern to the thermal properties. This may have been acceptable with yerterday's low power transistors and amplifiers; but with today's super power GaAs FET transistors, high power amplifiers; and a keen desire for the ultimate in reliability, the thermal considerations of the design must be studied in detail.

6.1 THERMAL RESISTANCE

The thermal resistance between two points R_{12} of a conductive system is expressed as

$$R_{12} = \frac{T_1 - T_2}{Pd} \quad {}^{o}C/W$$

where subscript order indicates the direction of heat flow, Pd is D.C. power dissipation in Watt.

A simplified heat transfer circuit for a cased semiconductor and heat sink system is shown in Figure 6.1.1. The circuit is valid only if the system is in thermal equilibrium (constant heat flow) and there are, indeed, single specific temperatures T_j, T_c, and T_s (no temperature distribution in junction, case and heat sink). Nevertheless, this is a reasonable approximation of actual performance.

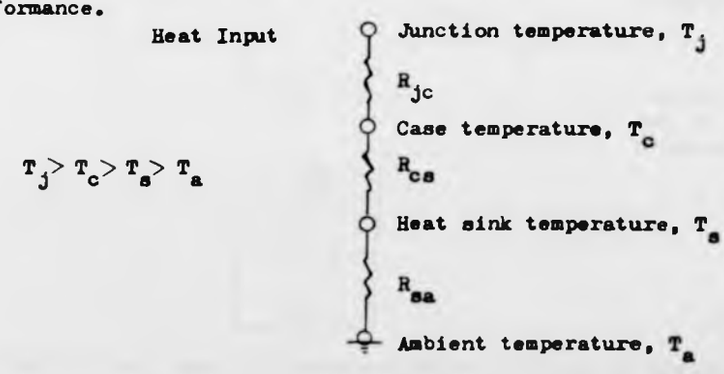


Figure 6.1.1 Semiconductor-Heat sink thermal circuit

6.2 Negative Resistance in the GaAs FETs Power Devices

The latest report on negative resistance in the GaAs FETs due to Gunn effect (1) is being used to analyse and predict the performance of the GaAs FET power amplifiers (2),(3).

It was found that the model suggested by Willing as shown in Figure 6.2.1 for the GaAs FETs is necessary but not sufficient as one has to ignore the thermal effect in the power devices.

Because the FETs performance and operational lifetime depend strongly on the temperature. A theoretical model and a measurement technique have been developed for determining FETs operating temperature and thermal resistance by Huang,et al.(4),(5).Therefore, it is found very useful to have resistance R_{th} , due to the thermal effect, added to the FET model in addition to Gunn effect as shown in Figure 6.2.1.

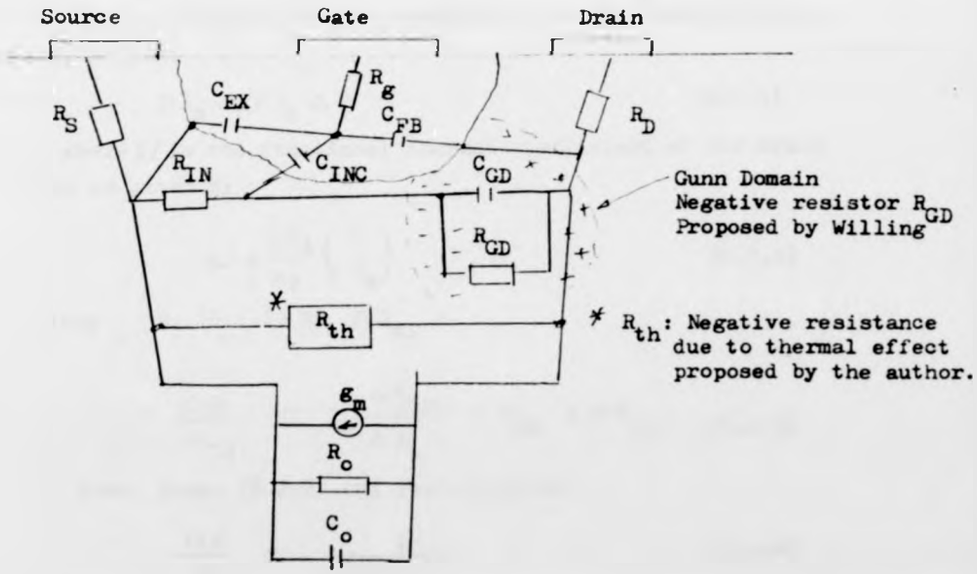


Figure 6.2.1 GaAs FET Intrinsic Model proposed by Willing [Ref (1)]

The following is the theoretical analysis of the negative resistance in the GaAs FET power device due to the thermal effect, which is similar to Todd's analysis for the silicon FET at very low frequency(6).

The drain to source voltage change is designated as ΔV_{ds} and the associated change in drain current as ΔI_c. Therefore the change in power dissipation is

$$\Delta P = (V_{ds} + \Delta V_{ds}) (I_d + \Delta I_d) - V_{ds} I_d$$

$$\Delta P = I_d \Delta V_{ds} + V_{ds} \Delta I_d + \Delta I_d \Delta V_{ds} \qquad (6.2.1)$$

The change in internal GaAs FET temperature ΔT that results is equal to product of ΔP and the channel to ambeient thermal resistance Θ, in degrees centigrade per watt,

$$\Theta = \frac{\Delta T}{\Delta P} \qquad \left({}^{\circ} C/\text{watt} \right) \qquad (6.2.2)$$

Assuming the change in operating current is entirely due to the change in internal channel temperature of the GaAs FET power device, so that

$$\Delta I_d = \mu I_d \Delta T \qquad (6.2.3)$$

where μ is the fractional thermal coefficient of the drain current as given by

$$\mu = \frac{\partial I_d}{\partial T} \left(\frac{1}{I_d} \right) \qquad (6.2.4)$$

Dividing Eq.(6.2.1) by ΔI_d :

$$\frac{\Delta P}{\Delta I_d} = I_d \frac{\Delta V_{ds}}{\Delta I_d} + V_{ds} + \Delta V_{ds} \qquad (6.2.5)$$

From Eqns. (6.2.2) and (6.2.3) yield

$$\frac{\Delta P}{\Delta I_d} = \frac{1}{\mu \Theta I_d} \qquad (6.2.6)$$

Substituting Eqns. (6.2.4) and (6.2.6) into (6.2.5):

$$\frac{1}{\frac{\partial I_d}{\partial T}\,\Theta} = I_d \frac{\Delta V_{ds}}{\Delta I_d} + V_{ds} + \Delta V_{ds} \qquad (6.2.7)$$

Let $R_{th} = \frac{\Delta V_{ds}}{\Delta I_d}$, the incremental FET output resistance at thermal equilibrium, from Eq. (6.2.7),

$$R_{th} = \left(\frac{1}{\Theta \frac{\partial I_d}{\partial T}} - V_{ds} - \Delta V_{ds} \right) / I_d \qquad (6.2.8)$$

Now, examine Eqn. (6.2.8), one can see that if $\frac{\partial I_d}{\partial T}$ is negative then R_{th} must be negative resistance.

With uniform doping in the semiconductor, the space charge-layer width W_{sb}, of the Schottky barrier is identical to that of a one-sided step p-n junction(7),

$$W_{sb} = \left[\frac{2 \epsilon_s (\phi_b - V_{gs})}{q N_d} \right]^{\frac{1}{2}} \qquad (6.2.9)$$

$$\phi_b = \phi_m - \phi_s - \frac{KT}{q} \qquad (6.2.10)$$

The term $\frac{KT}{q}$ arises from the contribution of the mobile carriers to the electric field(8).

From fundamental equations of junction FETs (9):

In the linear region:

$$I_d = \frac{W q u_n N_d d}{L} \left\{ V_{ds} - \frac{2}{3} \left(\frac{8 \epsilon_s}{q N_d d^2} \right)^{\frac{1}{2}} \left[(V_{ds} + \phi_b - V_{gs})^{3/2} - (\phi_b - V_{gs})^{3/2} \right] \right\} \qquad (6.2.11)$$

In the saturation region

$$I_{dsat} = \frac{W q u_n N_d d}{L} \left\{ \left(\frac{2}{3} \sqrt{\frac{8 \epsilon_s (\phi_b - V_{gs})}{q N_d d^2}} - 1 \right) (\phi_b - V_{gs}) + \frac{1}{3} \frac{q N_d d^2}{8 \epsilon_s} \right\} \qquad (6.2.12)$$

where

L,W and d designate the length, width and the thickness of the channel, respectively

N_d: the donor concentration in the channel region

q : the charge of an electron

ϵ_s: the reletive dielectric constant of GaAs meterial

u_n: the mobility of the electron in channel

V_{ds}: drain to source voltage

V_{gs}: gate to source voltage

$q\phi_m$ and $q\phi_s$: the work function of the metal and the semiconductor

ϕ_b: built-in voltage of the Schottky barrier

I_d : drain current

I_{dsat} : saturation drain current

K : Boltzmann's constant

If the density of the ionized donors remain essentially the same over a certain temperature range in n-type GaAs FET, then the pinch off voltage V_p is given as

$$V_p = \frac{qN_d d^2}{2\epsilon_s} \qquad (6.2.15)$$

which will be constant with temperature(7); however, the pinch off current I_p is given as

$$I_p = \frac{Wu_n q^2 N_d d^3}{6\epsilon_s L} \qquad (6.2.16)$$

will vary with temperature because of the mobility variation.

From Eqs. (6.2.9) to (6.2.12), the effect of the temperature on either I_d or I_{dsat} is mainly due to electron mobility u_n and the built-in potential of the Schottky barrier ϕ_b.

In an n-type semiconductor the velocity distribution is nearly Maxwellian(10), for isotropic scattering and constant free path length, therefore:

$$u_n = ql \left(\frac{8}{9\pi m_n^* KT}\right)^{\frac{1}{2}} \qquad (6.2.17)$$

where l: constant free path length at thermal equilibrium.

T: temperature

m_n^*: effective mass of an electron

From Eqns.(6.2.10) and (6.2.17),one can see that both quantities u_n and ϕ_b cause I_d and I_{dsat} to decrease with increasing temperature.

As an example, a 2.5 watts GaAs FET power device: MSC88010, was evaluated over an ambient temperature range from 0.0°C to 50°C. By keeping V_{ds}= 4 Volts, the drain to source current I_d was monitored while the chamber temperature T was varied. Table 6.2.1 is the measurement results for three different V_{gs} setting values (0.0,-0.5 and -1.5 Volts).

$\frac{\partial I_d}{\partial T}$ are the average values and R_{th} are the calculated using Eq.(6.2.8).

V_{gs} (Volts)	$\frac{\partial I_d}{\partial T}$ (mA/°C)	R_{th} (Ohms)
0.0	- 5.6	-6.7
-0.5	- 4.4	-10.0
-1.5	- 3.8	-15.0

Table 6.2.1 The Negative Resistance due to Thermal Effect for the MSC88010

D.C. characteristic measurement results for the MSC88010 are shown in Figure 6.2.3. An X-Y recorder is used in conjunction with a buffer circuit as shown in Figure 6.2.2.

For lower power device (MSC88001), any negative resistance can be hardly seen as shown in Figure 6.2.4.

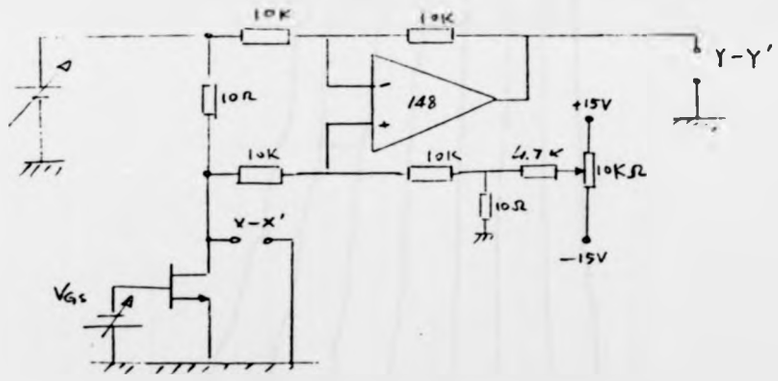


Figure 6.2.2 Buffer circuit of X-Y recorder for manually measuring static characteristics of power GaAs FET

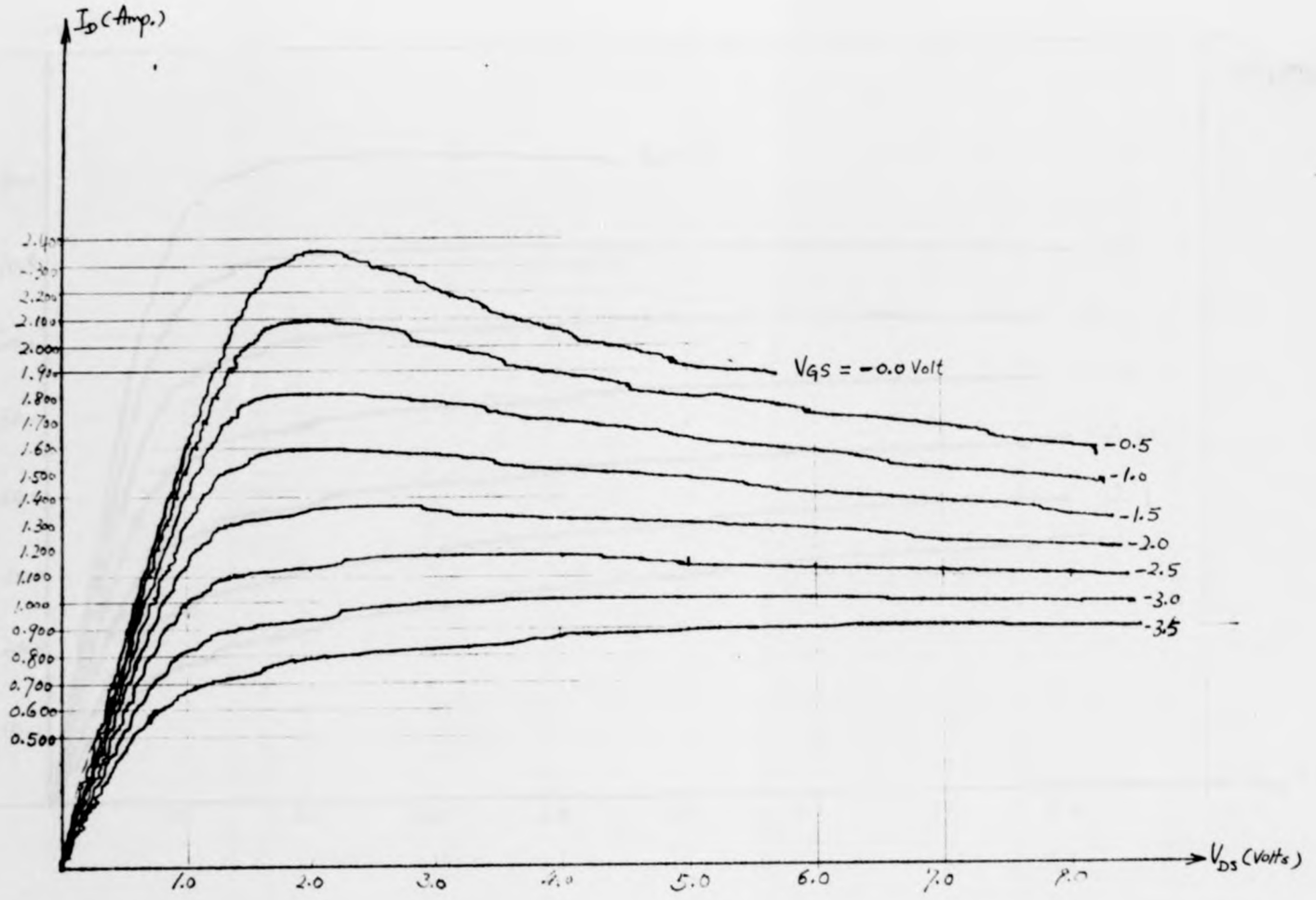


Figure 6.2.3. Measured Static I_{ds} vs. V_{ds} Characteristics for MSC88010

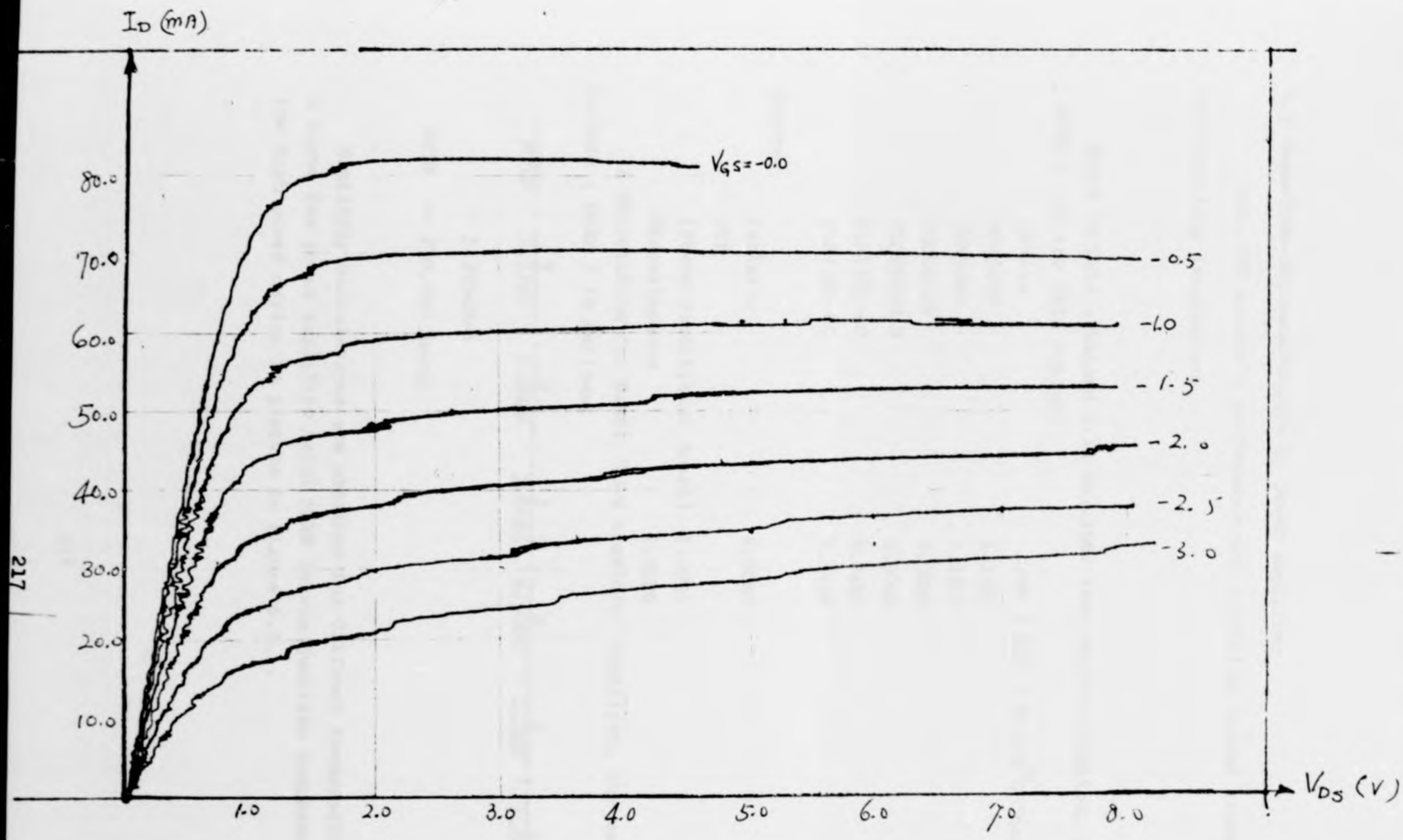


Figure 6.2.4 Measured Static I_{ds} vs. V_{ds} Characteristics for MSC88001

6.3 Mean-Time-Between-Failure of Power Amplifier

GaAs FET device's performance and operation depend strongly on the operating temperature.

Based on Data obtained till May,1982 from Fujitsu Limited, mean-time-to-failure (MTTF) for the FETs follow:

Device	MTTF (Hrs) @ 145°C Channel temperature
FSX51WF	1.13E7
FSX52WF	1.13E7
FLC081WF	4.00E6
FLC253MH-8	4.00E6
FLM7785-4C	3.84E6
FLM7785-8C	3.84E6

Others:

Isolator	6.50E6
PCB (Power Conditioner Board)	1.20E6
Miscellaneous	1.00E6

A calculation for 8-GHz, 10-W compleded amplifier, the mean-time-between-failure (MTBF) is follows:

$$\frac{1}{MTBF} = \frac{3}{1.13E7} + \frac{2}{4.00E6} + \frac{3}{3.84E6} + \frac{4}{6.50E6} + \frac{1}{1.2E6} + \frac{1}{1.00E6}$$

$$= 3.9954E\text{-}6$$

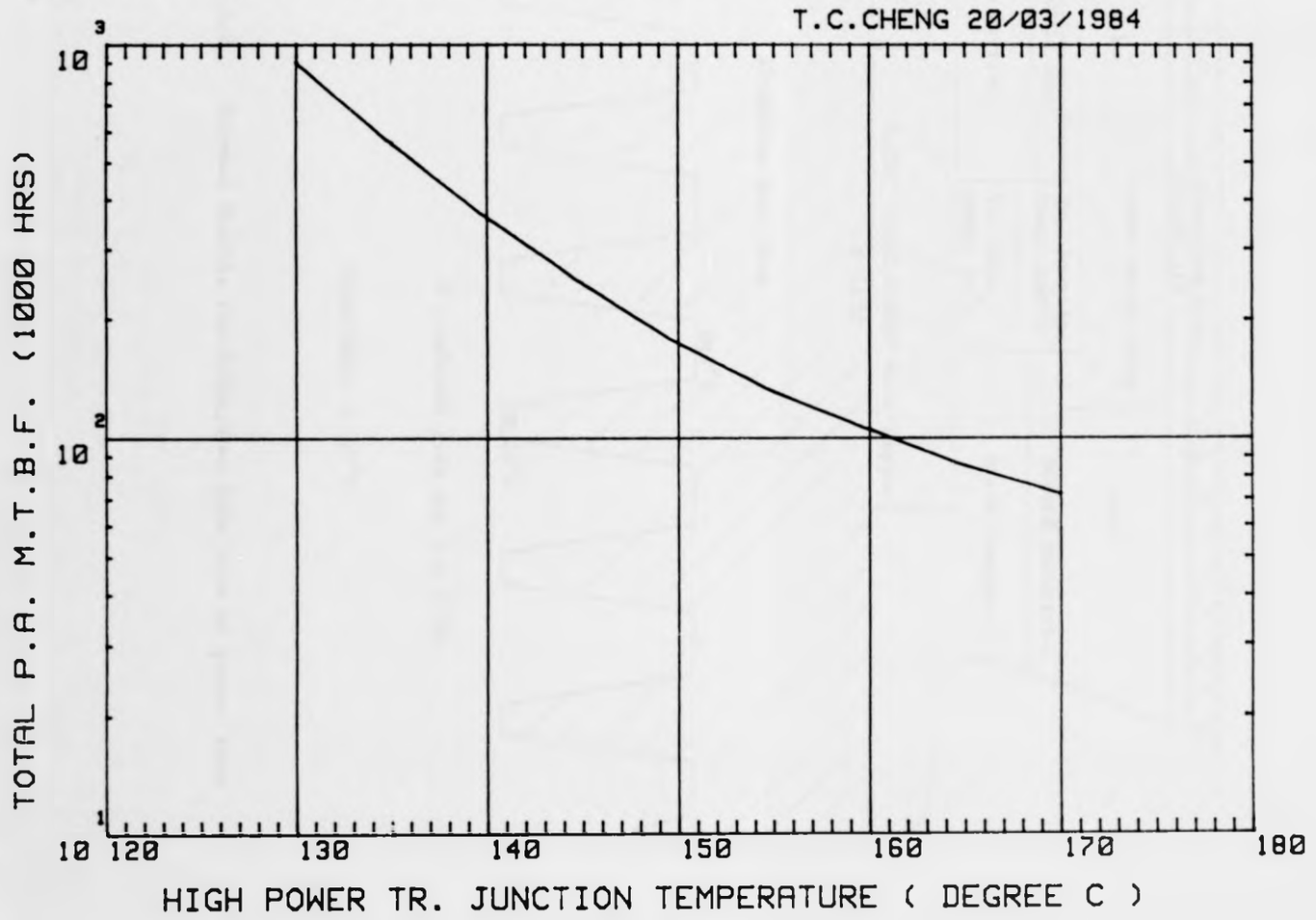
$$MTBF = 250{,}000 \text{ Hours}$$

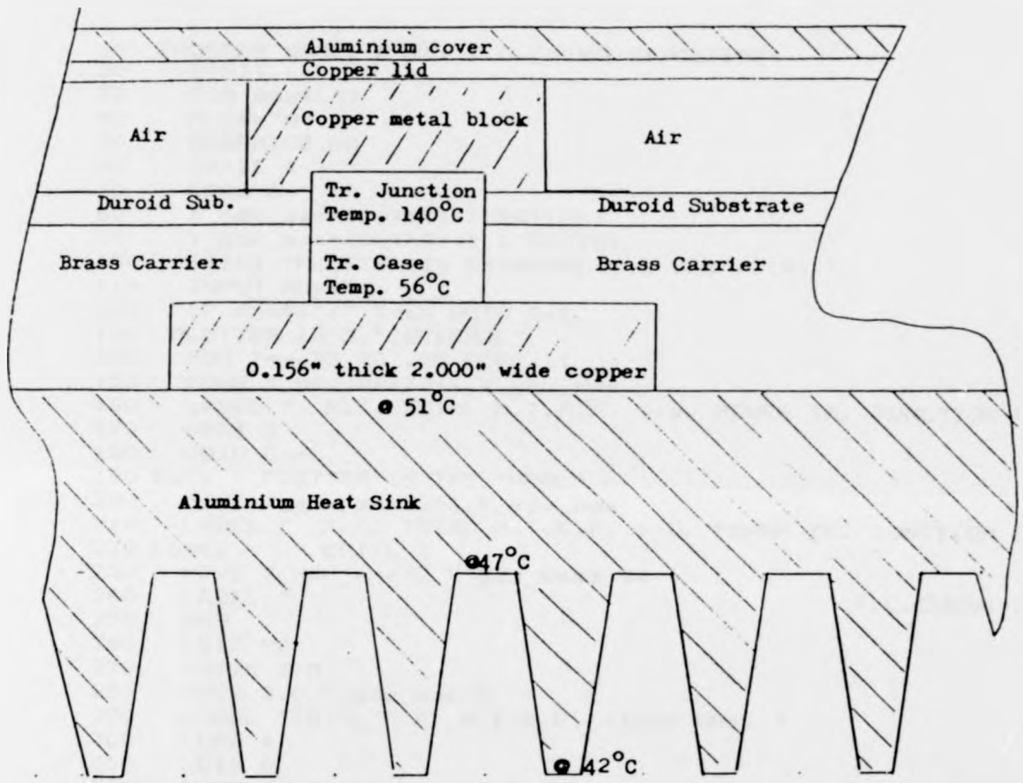
Similarly calculations are obtained for diffrent temperatures, and a curve for power amplifier total MTBF versus junction temperature of the high power device is plotted in Figure 6.3.1.

Figure 6.3.2 is the cross section profile of the SSPA where the high power device FLM7785-8C was located.

The temperature was measured on the prototype 8 GHz, 10 watt SSPA installed in the Northern Telecom's MD-3 digital microwave radio bay. The room temperature was 27°C, and the ambient temperature(the bay) was 37°C. The total DC power dissipation was 65 W, and the thermal resistance of the FLM7785-8C device was 4°C/W, with V_{ds}= 10 V and I_{ds}= 2.1 A. Hence, the temperature from the case to the junction of the transistor rose to 84°C. Now, with the case temperature at 56°C the actual junction temperature became 140°C, which corresponded to the total mean time between failure (MTBF) of the SSPA as 350,000 hours.

FIGURE 6.3.1 P.A. TOTAL M.T.B.F. v.s. POWER TR. JUNCTION TEMP.





T (ambient /the Bay) = 37°C

Room Temp. = 27°C

Figure 6.3.2 Thermal Profile for 8-GHz, 10-W SSPA with DC power : 65-W

6.4 Computer program listing for MTBF curve plotting

```
10! PROGRAM NAME: MTBF: T.C.CHENG 21/03/1984
20    GINIT
30    DIM Ans$[3]
40    Ans$="N"
50    GRAPHICS ON
60    CSIZE 4
70    LORG 6
80    X_gdu_max=100*MAX(1,RATIO)!
90    Y_gdu_max=100*MAX(1,1/RATIO)!
100   PRINT "PLOTTER IS EXTERNAL ? ( Y/N ) <N> "
110   INPUT Ans$
120   IF Ans$="Y" THEN GOTO Ext
130  PLOTTER IS 3,"INTERNAL"
140   FOR I=-.25 TO .25 STEP .1
150   MOVE X_gdu_max/2+I,Y_gdu_max
160   LABEL "  P.A. TOTAL M.T.B.F. v.s. POWER TR. JUNCTION TEMP. "
170   NEXT I
180   GOTO Cont
190 Ext:   PLOTTER IS 705,"HPGL"
200   MOVE X_gdu_max/2+I,Y_gdu_max
210   LABEL "  P.A. TOTAL M.T.B.F. v.s. POWER TR. JUNCTION TEMP. "
220 Cont:      CSIZE 3
230   MOVE X_gdu_max/2,Y_gdu_max*.94
240   LABEL "                                          T.C.CHENG 20/03/1984"
250   DEG
260   LDIR 90
270   CSIZE 3.5
280   MOVE 3.0,Y_gdu_max/2
290   LABEL "TOTAL P.A. M.T.B.F. (1000 HRS) "
300   LORG 4
310   LDIR 0
320   MOVE X_gdu_max/2,.07*Y_gdu_max
330   LABEL "HIGH POWER TR. JUNCTION TEMERATURE ( DEGREE C )"
340   VIEWPORT .1*X_gdu_max,.98*X_gdu_max,.15*Y_gdu_max,.9*Y_gdu_max
350   Xmin=120
360   Xmax=180
370   Xrange=Xmax-Xmin
380   Ymin=1
390   Ymax=4
400   Yrange=Ymax-Ymin
410   Dy=.1
420   WINDOW Xmin,Xmax,Ymin,Ymax
430   LINE TYPE 1
440   CLIP OFF
450   FOR Decade=Ymin TO Ymax
460      FOR Units=1 TO 1+8*(Decade<Ymax)
470         Y=Decade+LGT(Units)
480         MOVE Xmin,Y
490         IF Y=Decade THEN GOTO 520
500         DRAW 1.001*Xmin,Y
510         MOVE Xmax*.999,Y
```

```
520           DRAW Xmax,Y
530        NEXT Units
540     NEXT Decade
550     ! LABEL THE Y AXIS
560     LINE TYPE 1
570     FOR Y=Ymin TO Ymax STEP Dy*10
580        LORG 6
590        CSIZE 3
600        MOVE Xmin-Xrange*.03,Y
610        LABEL USING "#,K";"10"
620        CSIZE 2
630        LORG 1
640        MOVE Xmin-Xrange*.03,Y+Yrange*.01
650        LABEL USING "#,K";Y
660        NEXT Y
670        CLIP OFF
680        LINE TYPE 1
690        !
700        Xtick=Xrange*10
710        FOR Xxx=Xmin TO Xmax STEP 10
720         MOVE Xxx,Ymin
730         DRAW Xxx,Ymin*.995
740         MOVE Xxx,Ymax*1.005
750         DRAW Xxx,Ymax
760         NEXT Xxx
770         FOR X=Xmin TO Xmax STEP 10
780         MOVE X,Ymin
790         DRAW X,Ymax
800         NEXT X
810        CSIZE 3
820        LORG 3
830        FOR I=Xmin TO Xmax STEP 10
840        MOVE I,Ymin
850        LABEL USING "#,K";I
860        NEXT I
861        PENUP
870        MOVE 130,900
880     FOR I=1 TO 9
890     READ X,Y
900     PLOT X,LGT(Y)
910     CSIZE 2.5,.5
920     !LABEL X
930     NEXT I
940     PENUP
941     DATA 130,900
942     DATA 135,560
952     DATA 140,360
953     DATA 145,247
954     DATA 150,171
955     DATA 155,130
956     DATA 160,101
957     DATA 165,85
958     DATA 170,72
960     END
```

6.5 References:

1. Willing,H.A. et al.:" Modelling of Gunn-Domain Effects in GaAs FETs," Electronics Letters, 1st Sep., 1977 Vol.13, No.18.
2. Willing H.A. et al.:" A Technique for Predicting Large-Signal Performance of a GaAs MESFET," IEEE Transaction on Microwave Theory and Technique ,Vol. MTT-26,No.12,Dec,1978,pp.1017ff.
3. Rauscher,C. et al.:" Simulation of Nonlinear Microwave FET performance Using a Quasi-Static Model," ibid.,Vol.MTT-27, No.10, Oct.,1979,pp.834ff.
4. Huang,H.C. et al.:" Measuring Thermal Resistance in GaAs Power FETs," Microwave Syst. News,Oct. 1978,pp.105-108.
5. Siegal,B.S.:" A Proposed Method for Testing Thermal Resistance of MESFETs," ibid.,Nov. 1977,pp.67-70.
6. Todd,C.D.:" Negative Resistance in FETs: an Aid or an Ailment," Electronics, July 26,1965,pp.57ff.
7. Yang,Edward S.:" Fundamental of Semiconductor Devices," McGraw-Hill Book Company 1978,pp. 126.
8. Sze,S.M.:" Physics of Semiconductor Devices," John Wiley & Sons, Inc., 1969.
9. Grove,A.S. :" Physics and Technology of Semiconductor Devices," John Wiley and Sons, Inc., 1967
10. Aldert van der Ziel," Solid State Physical Electronics," Prentice-Hall Inc., Englewood Ciffs, New Jersey 1976.

CHAPTER 7 CONCLUSION

The RD-3 is Northern Telecom's long haul (6560 KM) digital microwave radio system, capable of transmitting and receiving a single bit stream of 91.04 Mbit/s rf channel giving it a capacity of 1344 vf channels. There are 12 rf channels operating in the 7.725 GHz to 8.275 GHz common carrier band. This digital radio has been in service since 1978 using a 10 watt TWT in the transmitter. In order to replace the TWT by a solid state power amplifier (SSPA), a prototype of a 10-W 8-GHz SSPA has been developed.

The SSPA is composed of five-unit amplifier modules. Module 1,3 and 4 consist of two cascaded amplifiers, each using Fujitsu FSX51WF and FSX52WF, FSX52WF and FLC081WF, FLC253MH-3 and FLM7785-4C devices respectively. Module 5 is a balanced amplifier module using two FLM7785-8C internally matched devices. Finally, Module 2 contains a PIN diode attenuator, serving as an rf element for automatic level control (ALC), in the overall amplifier.

The amplifier modules were designed using CAD techniques (Super-Compact^{TM}). Module 1,2,3 and 4 were designed as linear amplifiers. Power dividing and combining in module 5 were made with 3dB branch-type microstrip couplers using Golden-ratio searching optimization technique. It is interesting to note that the total circuit loss is only 0.8dB over 2.8 inches of physical length of module 5, including four DC block capacitors and two 40dB couplers for sampling the rf signal. Microstrip circuits were fabricated on 25 mil thick Duroid substrate having a relative dielectric constant of 10.2.

A constant gate voltage biasing network was adapted and optimized. It has already been shown, that by using a constant gate voltage biasing circuit, there is a considerable difference to the GaAS FET amplifier as far as linearity is concerned. By using FLM7785-8C device for example, due to the rf signal drift, the measured reverse-gate current was less than 0.5 ma in the constant gate biasing case, while with constant drain biasing, the current can go as high as 2.79 ma. The abundance of gate current in the latter case can be very damaging to the device as far as lifetime is concerned.

The SSPA was evaluated over a wide ambient temperature range from -10°C to 50°C under forced air cooling conditions.

The variation in the output power over the temperature range was 1.8dB maximum at the rated output power level.

The AM to AM conversion ratio was 0.375dB/dB and AM to PM conversion ratio, defined as delta-phase/delta-pin was 0.84°/dB. The third-order intermodulation distortion was also measured using the method described by Heiter. This method involved the injecting of two equal amplitude signals, 7790MHz and 8000MHz, separated in frequency by 10MHz. The extrapolated third-order intermodulation turned out to be 49dBm.

The GaAS FET devices overall performance and operational lifetime depend strongly on the operating temperature.

The total mean-time-between failure (MTBF) of the SSPA is 350,000 hours.

The prototype of the 8GHz, 10-W SSPA has been tested in the Northern Telecom's RD-3 bay. The results showed a residual bit error rate (BER), with an output power level of 40dBm to be 1.0×10^{-32} for the SSPA compared with 1.0×10^{-23} for the TWT.

PUBLICATIONS

I. " Nonlinearity in GaAs FET Power Amplifiying Devices "
Electronics Letters 13th September 1984 Vol.20 No.19
pp.788-790.

II. " Automatic Non-linearity Measurements of GaAs FET Power Devices "
Submitted to the 4th Meeting of the Automated R.F. and Microwave Measurement Society (ARMMS) at York University, on 27th September,1984.

III. " ·8 GHz, 10 W Solid-State Power Amplifier for Microwave Digital Radio "
Electronics Letters 31th January 1985 Vol.21 No.3
pp. 110-111.

NONLINEARITY IN GaAs FET POWER AMPLIFYING DEVICES

Indexing terms: Microwave circuits and systems, Semiconductor devices and materials

Modern microwave communication systems rely heavily on the linearity of output stages incorporating GaAs FET power amplifying devices. This letter describes a system for the automatic nonlinearity measurement in such devices of gain and phase angle as functions of input power level and frequency, with results leading to significantly improved system performance.

It is well known that in a solid-state amplifier, as used for the power output stage of a microwave radio communication system, spurious conversion from AM to AM and from AM to PM arising within the amplifier can contribute significantly to group delay distortion, differential gain, differential phase and consequently to intermodulation distortion.[1-3] The amount of spurious conversion introduced is known to depend on the level of operation and to be a function of the operating frequency. The phenomenon is closely linked with changes in gain (delta gain) and phase angle (delta phase). These have been studied for GaAs FET microwave power amplifying devices as functions of power level and frequency, using the automated system illustrated in Fig. 1.

In the measurement of gain, the output signal from a test device (DUT) is compared as a ratio with that from a reference channel in a heterodyne system. A similar arrangement is used for phase angle measurements, IF signals being compared in a phase detector. The system has been automated with the aid of a computer (hp 9845 or 9816) in conjunction with a programmable sweep oscillator (hp 8350A) plus broadband plug-in (hp 83592A). These are used in the generation of a levelled signal of appropriate magnitude, phase and frequency, a sample of which is fed into the reference channel of a harmonic frequency convertor (hp 8411A), whose test channel receives an attenuated version of the signal transmitted by the DUT. Power levels at both input and output of the DUT are monitored by programmable power meters (hp 436A), and results are displayed either via a plotter (hp 7225B) or printer (hp 82905B).

Measurements are accomplished by programming the sweep oscillator to give a succession of frequencies and to step the power level within the required dynamic range. Six A/D convertor channels are used in total for the input of information to the computer, covering gate and drain currents and voltages, together with the magnitude and phase of signals transmitted by the DUT.

In order to accommodate repeatability errors, each measurement is performed up to ten times, and the data collected in the form of a matrix (A). The number of rows correspond to the number of repetitions, the columns similarly corresponding to the stepped power levels. Where changes only in gain or phase are required, i.e. delta gain or delta-phase, the first column of matrix (A) may be offset to zeros, resulting in a matrix (B), in which corresponding elements are related by

$$b_{jk} = a_{jk} - a_{j1}$$

where

j = row number = 1, r

k = column number = 1, s

Taking the sum of elements in each column and dividing by the number of measurement repetitions r yields the average data for each test point in the form of a row matrix (C), where

$$C = (0, c_2, c_3, \ldots, c_k, \ldots, c_s)$$

and

$$c_k = \left(\sum_{j=1}^{r} b_{jk}\right)\Big/ r$$

Designating by C the row matrix pertaining to calibration and by M the corresponding matrix for a DUT, the difference matrix (D), given by

$$D = (0, m_1 - c_1, m_2 - c_2, \ldots, m_k - c_k, \ldots, m_s - c_s)$$

describes the deviation from linearity of the DUT. Hence, using appropriate scaling factors to convert from digitised binary numbers to analogue quantities and incorporating power meter readings, all of the required nonlinearity information may be computed. Software was devised such as to allow for a series of calibration subroutines to be followed by appropriate measurement subroutines.

The system is useful for selecting devices appropriate to a particular application, but one major and unexpected bonus from the investigation is revealed by the comparison of results in Figs. 2–5. These are for delta gain and delta phase as functions of output power and frequency and relate to Fujitsu GaAs FET devices operated under conditions of constant voltage bias as well as the more usual constant current bias. It is to be noted that performance in relation to both gain and phase is significantly improved by using a constant voltage bias.

The reduction in delta gain may be as much as 0.5 dB, while delta phase at 2 dB gain compression may be reduced by up to 6° for output powers approaching 10 W at 8 GHz.

Additionally, advantages for constant voltage bias have been observed in terms of reverse gate current and overall power dissipation. It is possible to gain an understanding of the reasons for the improved performance by considering the device output characteristics in conjunction with the dynamic load line.

This reveals a greater symmetry in the positive and negative swings of the drain current for the constant voltage bias case, since with constant current bias a shift in the mean-gate source voltage occurs, leading to a cutoff situation persisting for a greater proportion of the cycle than is affected by saturation, thereby introducing a higher degree of nonlinearity.

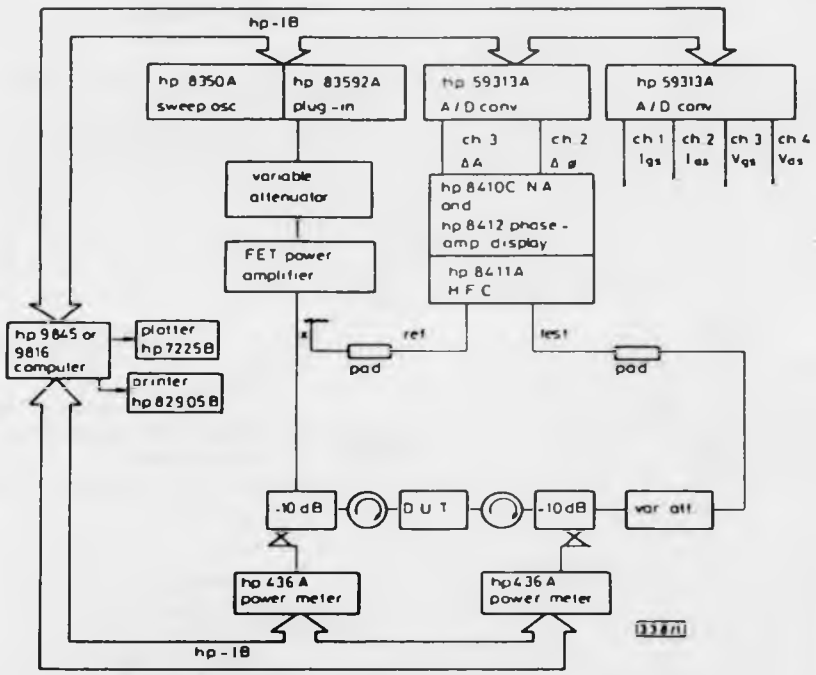


Fig. 1 *Automatic delta-gain and delta-phase measurement equipment*

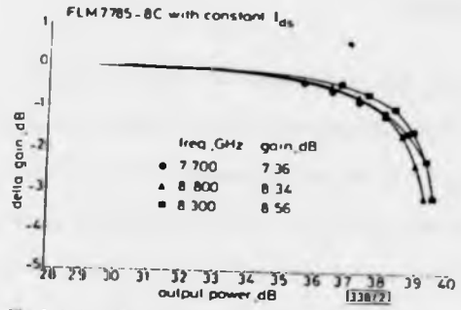


Fig. 2 *Delta gain against output power (constant I_{ds})*

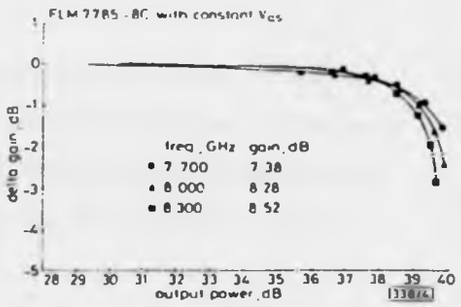


Fig. 4 *Delta gain against output power (constant V_{gs})*

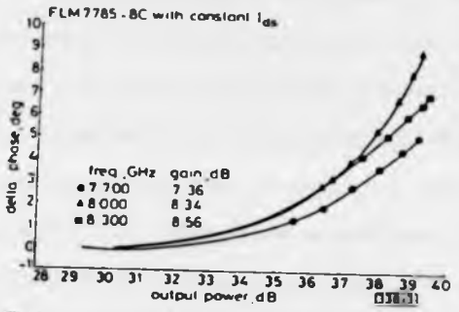


Fig. 3 *Delta phase against output power (constant I_{ds})*

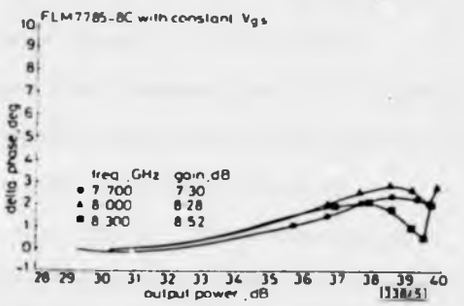


Fig. 5 *Delta phase against output power (constant V_{gs})*

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31st July 1984

References

1 AHMED, M. J.: 'Swept frequency AM to PM conversion measurement', *Microwave J.*, 1977, **20**, pp. 58–59

2 GARRISON, G. J.: 'Intermodulation distortion in frequency division multiplex FM systems—tutorial summary', *IEEE Trans.*, 1968, **COM-16**, pp. 289–303

3 SPROUL, P. T., and GRIFFITHS, H. D.: 'The broad-band radio transmitter and receiver', *Bell Syst. Tech. J.*, 1961, **XL**, pp. 1543–1547

Automatic Non-linearity Measurements of GaAsFET Power Devices

by H.V. Shurmer and T.C. Cheng

SUMMARY

Modern microwave communication systems rely heavily on the linearity of output stages incorporating GaAsFET power amplifying devices. This paper is devoted to the description of a system for the automatic measurement of deviations from linearity in such devices of both gain and phase angle as functions of input power level and frequency.

In the measurement of gain, the output signal from a test device (D.U.T.) is compared as a ratio with that from a reference channel in a heterodyne system. A similar arrangement is used for phase angle measurements, i.f. signals being compared in a phase detector. The system has been automated with the aid of a computer (hp 9845 or 9810) in conjunction with a programmable sweep oscillator (hp 8350A) plus broad-band plug-in (hp 83592A). These are used in the generation of a levelled signal of appropriate magnitude, phase and frequency, a sample of which is fed into the reference channel of a harmonic frequency converter (hp 8411A), whose test channel receives an attenuated version of the signal transmitted by the D.U.T. Power levels at both input and output of the D.U.T. are monitored by programmable power meters (hp 436A) and results are displayed either via a plotter (hp 7225B) or printer (hp 82905B).

Measurements are accomplished by programming the sweep oscillator to give a succession of frequencies and to step the power level within the required dynamic range. Six A/D converter channels are used in total for the input of information to the computer, covering gate and drain currents and voltages, together with the magnitude and phase of signals transmitted by the D.U.T.

In order to accommodate repeatability errors, each measurement is performed up to 10 times and the data collected in the form of a matrix(A). The number of rows corresponds to the number of repetitions, the columns similarly corresponding to the stepped power levels. Where changes only in gain or phase

are required, i.e. delta-gain or delta-phase, the first column of matrix(A) may be off set to zeros, resulting in a matrix(B), in which corresponding elements are related by

$$b_{jk} = a_{jk} - a_{j1}$$

where j = row number = 1,r

k = column number = 1,s

Taking the sum of elements in each column and dividing by the number of measurement repetitions, r, yields the average data for each test point in the form of a row matrix(C), where

$$C = (0, c_2, c_3, \ldots, c_k, \ldots c_s)$$

and $$c_k = \left(\sum_{j=1}^{r} b_{jk}\right)/r.$$

Designating by C the row matrix pertaining to calibration and by M the corresponding matrix for a D.U.T., the difference matrix(D), given by

$$D = (0, m_1 - c_1, m_2 - c_2, \ldots, m_k - c_k, \ldots, m_s - c_s)$$

describes the deviation from linearity of the D.U.T. Hence, using appropriate scaling factors to convert from digitized binary numbers to analogue quantities and incorporating power meter readings, all of the required non-linearity information may be computed.

BASIC was used as the programming language in implementing the procedures outlined and the programme arranged largely as sub-routines from the viewpoint of versatility. Results are given for measurements on individual GaAsFET devices. It has been found that a simple biassing circuit delivering a constant gate voltage has significant advantages for linearity compared with the more usual form of network giving constant drain current, one particular type of device (Fujitsu FLM7785-8c) being improved in terms of delta-gain by up to 0.5 dB and in delta-phase by up to 6 degrees, for output powers approaching 10 watts at 8 GHz.

8 GHz, 10 W SOLID-STATE POWER AMPLIFIER FOR MICROWAVE DIGITAL RADIO

Indexing terms: Microwave circuits and systems, Amplifiers

An 8 GHz, 10 W GaAs FET prototype power amplifier has been developed to replace the TWT in the Northern Telecom's digital microwave radio system. For a single bit stream of 91·04 Mbit/s, the residual bit error rate at 40 dBm output level was $1·0 \times 10^{-11}$ compared with $1·0 \times 10^{-13}$ for TWT; the AM/AM conversion ratio was 0·375 dB/dB and AM/PM was 0·84°/dB. The total mean time between failure of the amplifier was 350 000 h.

The RD-3 is Northern Telecom's long-haul (6560 km) digital microwave radio system, capable of transmitting and receiving a single bit stream of 91·04 Mbit/s RF channel, giving it a capacity of 1344 VF channels. There are 12 RF channels operating in the 7·725–8·275 GHz common carrier band.[1,2] This digital radio has been in service since 1978 using a 10 W TWT in the transmitter. In order to replace the TWT by a solid-state power amplifier (SSPA), a prototype of a 10 W, 8 GHz SSPA has been developed.

The SSPA is composed of five unit amplifier modules. Modules 1, 3 and 4 consist of two cascaded amplifiers, each using Fujitsu FSX51WF and FSX52WF, FSX52WF and FLC081WF, FLC253MH-8 and FLM7785-4C devices, respectively. Module 5 is a balanced amplifier module using two FLM7785-8C internally matched devices. Finally, module 2 contains a PIN diode attenuator, serving as an RF element for automatic level control (ALC) in the overall amplifier.

Fig. 1 shows the block diagram for the seven-stage 10 W

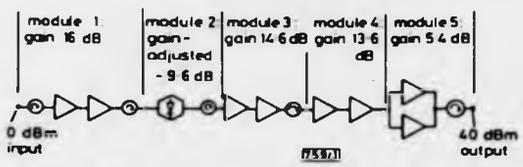

Fig. 1 *Block diagram for seven-stage 10 W solid-state power amplifier*

amplifier. Fig. 2 is the top view of the SSPA with the housing cover removed. The amplifier modules were designed using CAD techniques (Super-Compact™). Modules 1–4 were designed as linear amplifiers. Power dividing and combining in module 5 were performed with 3 dB branch-type microstrip couplers using the golden-ratio searching optimisation technique.* It is interesting to note that the total circuit loss is only 0·8 dB over the 2·8 in length of module 5, including four DC block capacitors and two 40 dB couplers for sampling the RF signal. Microstrip circuits were fabricated on 25×10^{-3} in-thick Duroid substrate with a relative dielectric constant of 10·2.

A constant gate voltage biasing network was adopted and optimised. It has already been shown[3] that by using a constant gate voltage biasing circuit makes a considerable difference to the GaAs FET amplifier as far as linearity is concerned. Using the FLM7785-8C device, for example, due to the RF signal drift, the measured reverse gate current was

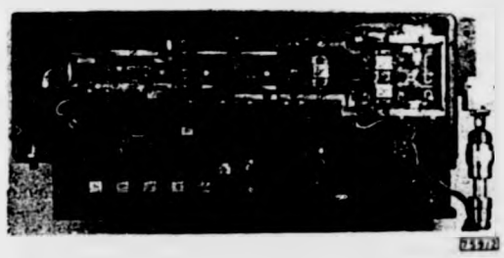

Fig. 2 *Photograph of the prototype 10 W solid-state power amplifier*

less than 0·5 mA in the constant gate biasing case, while, with constant drain biasing, the current can go as high as 2·79 mA. The abundance of gate current in the latter case can be very damaging to the device as far as lifetime is concerned.

* CHENG, T. C.: (unpublished work)

The SSPA was evaluated over a wide ambient temperature range from −10°C to 50°C under forced air cooling conditions. Fig. 3 shows the output power against frequency

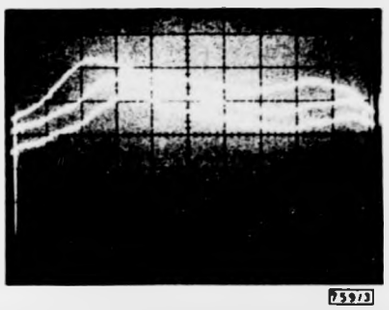

Fig. 3 *Output power response of the SSPA over a wide ambient temperature range*
Top trace: at −10°C; centre trace: at 27°C; bottom trace: at 50°C
Vertical scale: 1 dB/div. Reference at centre line is calibrated at 40 dBm
Horizontal scale: 60 MHz/div, from 7·7 to 8·3 GHz

response at three temperatures: −10°C, 27°C and 50°C. The variation in the output power over the temperature range was 1·8 dB maximum at the rated output power level. Power output against power input is shown in Fig. 4, when the output power level was at 40 dBm and the ALC circuit was in the OFF position, the corresponding input power was −12 dBm at 8 GHz. The AM/AM conversion ratio, defined as $\Delta P_{out}/\Delta P_{in}$, was 0·375 dB/dB, and the AM/PM conversion ratio, defined as Δ phase/ΔP_{in}, was 0·84°/dB. The third-order intermodulation distortion was also measured using the method described by Heiter.[4] This method involved the injecting of two equal amplitude signals, 7990 MHz and 8000 MHz, separated in frequency by 10 MHz. The extrapolated third-order intermodulation intercept turned out to be 49 dBm.

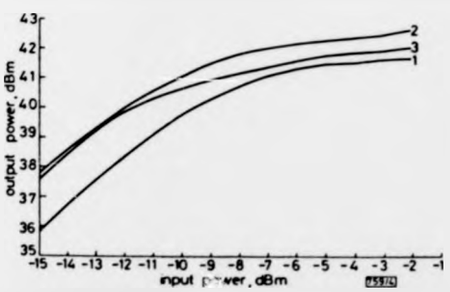

Fig. 4 *Output power against input power of the SSPA*

	Frequency, GHz	Gain, dB
Curve 1	7·700	50·82
Curve 2	8·000	52·79
Curve 3	8·300	52·56

The GaAs FET device's overall performance and operational lifetime depend strongly on the operating temperature. A theoretical model and a measurement technique have been developed by Huang *et al.*[5,6] to determine the FET operating temperature and thermal resistance. The temperature was measured on the prototype 8 GHz, 10 W SSPA installed in the Northern Telecom's RD-3 digital microwave radio bay. The room temperature was 27°C, and the ambient temperature (the bay) was 37°C. The total DC power dissipation was 65 W, and the thermal resistance of the FLM7785-8C device was 4°C/W, with V_{ds} = 10 V and I_{ds} = 2·1 A. Hence, the temperature from the case to the junction of the transistor rose to 84°C. The junction temperature of the transistor reached 140°C, which corresponded to the total mean time between failure (MTBF) of the SSPA as 350 000 h. The residual bit error rate (BER), with an output power level of 40 dBm, was $1·0 \times 10^{-32}$ for the SSPA compared with $1·0 \times 10^{-23}$ for the TWT.

Acknowledgment: The author wishes to thank Bell-Northern Research for permission to publish this letter.

T. C. CHENG *26th November 1984*

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References

1 'RD-3 digital microwave radio', Northern Telecom Practice, Section 415-3000-100, issued 10th Oct. 1981, pp. 1–28
2 ANDERSON, C. W., and BARBER, S. G.: 'Modulation considerations for a 91 Mbit/s digital radio', *IEEE Trans.*, 1978, **COM-26**, (5)
3 CHENG, T. C., and SHURMER, H. V.: 'Nonlinearity in GaAs FET power amplifying devices', *Electron. Lett.*, 1984, **20**, pp. 788–790
4 HEITER, G. L.: 'Characterization of nonlinearity in microwave devices and system', *IEEE Trans.*, 1973, **MTT-21**, pp. 797–804
5 HUANG, H. C., SECHI, F. N., and NAPOLI, L. S.: 'Measuring thermal resistance in GaAs power FETs', *Microwave Syst. News*, Oct. 1978, pp. 105–108
6 SIEGAL, B. S.: 'A proposed method for testing thermal resistance of MESFETs', *ibid.*, Nov. 1977, pp. 67–70